

LOW-COST IMPLEMENTATION OF HIGH-RESOLUTION PWM SCHEME FOR ADJUSTABLE SPEED DRIVES

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ABSTRACT

The performance and cost of an adjustable speed drive (ASD) depends largely on the PWM schemes and the implementation technique. In this paper, a new PWM implementation technique is proposed, where, an external ROM based circuit generates real time PWM patterns for the inverter on carrier cycle basis. Due to carrier cycle basis implementation, the scheme needs lesser external memory. The computational burden on the processor reduces much in the proposed scheme due to the use of Look-Up-Table (LUT), having little interaction with the processor and hence a low cost, low speed processor is capable of generating high-resolution PWM patterns using advanced PWM strategies. The proposed scheme offers wide range operation of an ASD with high resolution PWM implementable with a moderate speed processor, providing high performance at low cost.

1. INTRODUCTION

Pulse Width Modulation (PWM) techniques of various forms are available in the literature for the control of voltage, frequency and spectral distribution of static inverters [1]. PWM techniques are used in power inverters and ASD's ranging from fractional horsepower to up to several thousand hp applications. Microprocessors are used for implementation of PWM schemes efficiently [2]. The PWM switching points are computed on-line and the real time PWM patterns are realized using the μ P, I/O interfaces and Programmable Timers [3]. In such a case, processor performs huge computation. Hence high-speed processor, with large memory, is required for the implementation. In contrast, programmed PWM implementation [4], [5] using ROM-based LUT, involves off-line calculation; thus requiring less computation time. The conventional ROM based implementation requires huge memory for generating high-resolution PWM patterns.

In this paper, a memory minimized novel LUT based implementation scheme is proposed that is capable of generating high-resolution PWM patterns for wide operating range. The implementation is done using a low cost processor and simplified hardware that makes it attractive for commercial applications in Adjustable Speed Drives (ASD) and Uninterrupted Power Supplies (UPS).

2. ANALYSIS OF REGULAR SAMPLED PWM

In the regular sampled PWM (RSPWM), the PWM pulse widths are calculated on carrier cycle basis [6]. The amplitude of the reference sine wave modulates the width of a pulse. The harmonic spectrum of RSPWM contains the fundamental, and the harmonics of carrier frequency. The amplitude of the fundamental is determined by the modulation index, M defined as, $M = 2V_m/V_s$, where, V_m is the peak value of the fundamental and V_s is the DC supply voltage of the inverter.

2.1 Determination of PWM Pulse Widths

Generally, the switching points of the PWM pulses can be obtained from the modulation of a sinusoidal modulating signal with a high frequency triangular carrier signal [6]. The modulating function is considered as a stepped sine wave having constant magnitude within a carrier period. Fig. 1 shows the calculation procedure of the PWM pulse in detail for the n^{th} PWM pulse. The sampling instant for the n^{th} sample is $t_\delta + (n-1)T_c$, where, t_δ is the delay time of the first sampling from the starting point. At $t_\delta + (n-1)T_c$ instant, the modulating reference is, $A_m \sin \omega \{t_\delta + (n-1)T_c\}$ and is represented by the length CD as shown in Fig. 1. From Fig. 1,

$$BD = \frac{T_c}{4} \times \frac{A_m \sin \omega \{t_\delta + (n-1)T_c\}}{A_c} \quad (1)$$

The total pulse width at the n^{th} sample is given by,

$$t_w = 2(OA + BD) = 0.5T_c \left[1 + M \sin\{\omega\{t_\delta + (n-1)T_c\}\} \right] \quad (2)$$

where, $M = A_m/A_c$, is called the modulation index. Now considering N number of carrier cycles in a fundamental period, one can write $\omega NT_c = 2\pi$. With $t_\delta = 0$, (2) can be written as,

$$t_w = 0.5T_c \left[1 + M \sin\{(n-1)2\pi/N\} \right] \quad (3)$$

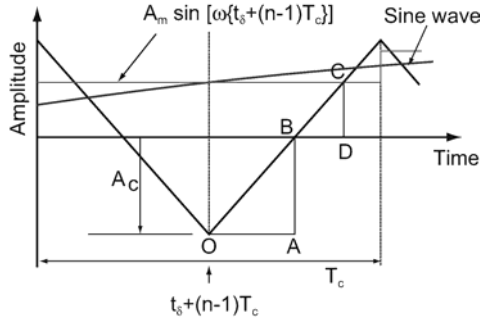


Fig. 1 Switching point calculation procedure for regular sample PWM from sampled reference waveform.

2.2 Pulse Width Modulation in Sampled Domain

Let K_c be the total number of samples in a carrier period (T_c) and Δt be the sampling interval. Hence, $\Delta t = T_c / K_c$. Now, in sample domain K_c samples corresponds to the period of a carrier cycle. The pulse width of the PWM pulse in sample domain is obtained by dividing both sides of (3) by Δt ,

$$t_w / \Delta t = (T_c / 2\Delta t) \left[1 + M \sin\{(n-1)2\pi/N\} \right]$$

or, $K_w = K_c / 2 + M_s \sin(n-1)2\pi/N$ (4)

where, $K_c = t_w / \Delta t$ and $M_s = (MK_c) / 2$ is the modulation tag. At 100% modulation, $M_s = K_c / 2$. Hence, K_w in (4) can have a maximum value of K_c .

2.3 Duty Tags

The duty tag is the number that corresponds to the duty cycle of a PWM pulse. Considering the maximum value of duty tag be $K_c / 2$, the modulation tag for phase A, B, C of PWM pattern would be,

$$D_a = \left[\frac{K_c}{2} + M_s \sin(n-1) \frac{2\pi}{N} \right] / 2 \quad (5)$$

$$D_b = \left[\frac{K_c}{2} + M_s \sin\left\{ (n-1) \frac{2\pi}{N} - \frac{2\pi}{3} \right\} \right] / 2 \quad (6)$$

$$D_c = \left[\frac{K_c}{2} + M_s \sin\left\{ (n-1) \frac{2\pi}{N} - \frac{4\pi}{3} \right\} \right] / 2 \quad (7)$$

2.4 Formation of PWM patterns in Sample Domain

PWM pulses for three phases for the n^{th} carrier cycle are shown in Fig. 2. The PWM pulse widths in

time domain are t_{wA} , t_{wB} and t_{wC} for phases A, B and C respectively. The PWM pulse for phase A in digital form is realized by scanning K_c samples upto the T_c period. The samples up to $(T_c/2 - t_{wA}/2)$ are assigned to be LOW and the rest of the samples up to $T_c/2$ are assigned HIGH. Again, from $T_c/2$ to $(T_c/2 + t_{wA}/2)$ the samples are assigned HIGH and the rest of the samples up to T_c are assigned LOW. Similarly the PWM pattern for the other phases can be formed.

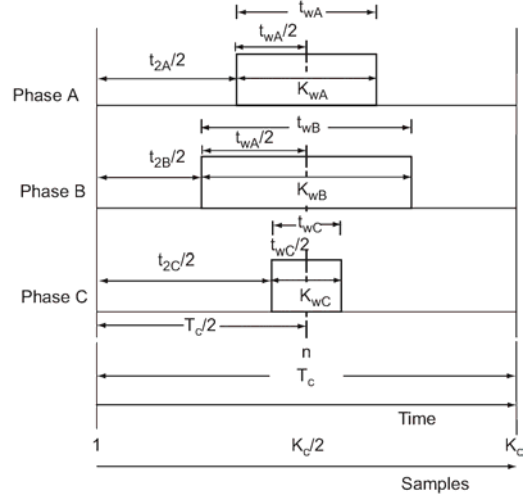


Fig. 2 PWM pulse patterns for one carrier cycle for phase A, phase B and phase C

3. PWM PATTERN GENERATION

The functional blocks of the real-time PWM pattern generation circuit is shown in Fig. 3. The schematic consists of six EPROMs and two counters. The six EPROMs are arranged in two stages; each stage consists of three EPROMs, one for each phase. These two EPROM stages are cascaded, i.e. first one addresses the second. Each of the EPROM stages is clocked by individual counters. These two counters are mutually dependent.

PWM pulse patterns having 128 different duty cycles ranging from 0% to 100% are stored in the last stage EPROMs. Each pattern (having T_c duration) corresponds to 256 samples. These samples are scanned over a carrier period by a 'Counter 2' to generate the real time PWM waveform in the EPROM data bus. A timer, at the required frequency, clocks the 'Counter 2' that produces a ripple carry (RC) when it finishes counting 255. This RC acts as the clock input of the first stage EPROMs 'Counter 1'. The count limit of this counter is determined by the input N of the first stage EPROM. The first set of EPROMs has pre-calculated PWM pulse duties for the fundamental period, consisting of different number of carrier pulses. Each EPROM of this set is scanned by three inputs: (a) The carrier pulse number n , which comes from 'Counter 1', (b) A tag number

N_s corresponding to the total number of carrier pulses in a fundamental period, N , which is set by the microcontroller, (c) Modulation tag M_s , which is also set by the microcontroller depending on the load requirement.

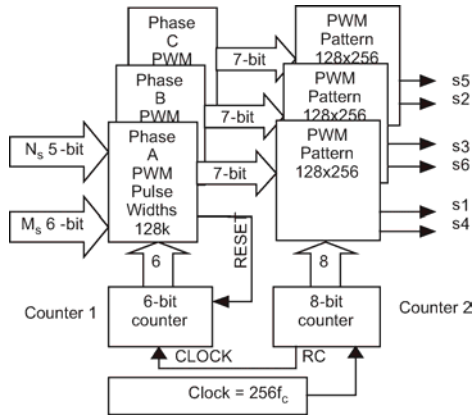


Fig. 3 External hardware for generating real time PWM patterns for three-phase inverter.

Once the microcontroller chooses a definite value for N_s and M_s for generating a fundamental period, only the magnitude of n will increment at each clock pulse of the ‘Counter 1’. Hence, the address of the first stage EPROMs is incremented with the counts of the ‘Counter 1’. At any instant, the counted number of the ‘Counter 1’ dictates the carrier pulse number. After the ‘Counter 1’ counts N , it is reset by a pulse from the data bit $D7$ prestored in the $(N+1)^{th}$ location, thus limiting ‘Counter 1’s counting by N . At each of the n count by ‘Counter 1’, the duty tag Dn is put in the data bus ($D0-D6$) of the first EPROMs set.

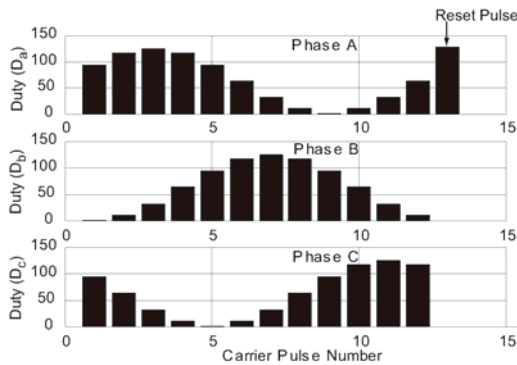


Fig. 4 PWM pulse duties for different carrier periods when $N=12$.

Typical PWM duty tags generated by proposed scheme for $N=12$ and $M_s=127$ is shown in Fig. 4. The indicated reset pulse is used to reset ‘Counter 1’ in Fig. 4, for starting next fundamental cycle. The lines ($D0-D6$) from this first set of EPROMs are connected to the upper 7-bit lines of the second set EPROMs that contains the PWM patterns for the pointed duty tag Dn in consecutive 256 memory

addresses, containing 1’s or 0’s required to construct a PWM pulse for that carrier period. Thus, for generating an output voltage of frequency f , the required clock frequency for ‘Counter 1’, which is the carrier frequency for the generated PWM pattern, will be $f_c = fN$ and ‘Counter 2’s required frequency will be $f_s = 256f_c$. By nature of the proposed scheme, the processor sets only the N and M_s values and can update them asynchronously.

4. ASD IMPLEMENTATION

The ASD needs variable voltage outputs at variable frequency operation. For generating output voltages at different frequencies, the fundamental period is set to be made of variable number of carrier periods. If carrier period is kept fixed, higher the number of carrier pulses required in forming a fundamental period, the lower will be the output frequency.

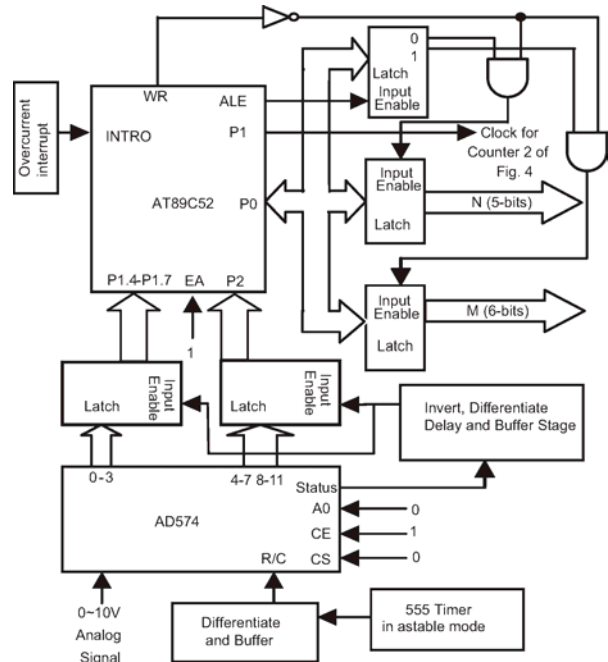


Fig. 5 Schematic and Block Diagram Arrangement for implementation of the proposed scheme in ASD.

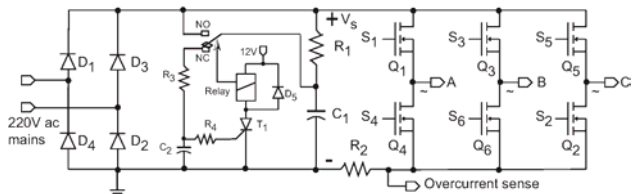


Fig. 6 The converter and inverter section of the ASD along with charging control circuitry.

The control part of the ASD scheme is shown in Fig. 5. The ASD is driven from a single-phase ac supply to suit most commercial applications. The single-phase ac supply is converted to DC by a

bridge rectifier and then fed to the power inverter designed with MOSFET switches as shown in Fig. 6.

The scheme is designed to drive a 500W 3-phase induction motor at variable speed ranging from 150 rpm to 5000 rpm. To achieve smooth speed change, the fundamental frequency is varied at small steps. The drive is operated in v/f control mode upto the base speed of 1500 rpm. After base speed, the drive is operated in variable frequency mode only. In the variable frequency mode, the number of PWM pulses in a fundamental period is fixed, but the frequency is varied by changing the clock frequency f_s by the built in timer of AT89C52. The speed command for the ASD is obtained from an analog potentiometer that gives an output voltage of 0V to 10V. The analog speed reference is converted to 12-bit binary format by the ADC AD574 and fed to AT89C52 as the digital speed reference.

5. SIMULATION AND RESULTS

The PWM scheme is simulated to evaluate its performance. For simulation, the motor current is taken as 1.7A and the motor equivalent impedance is taken into consideration in determining the proper modulation index and frequency of operation. Fig. 7 shows the simulation results for the ASD scheme with an induction motor load of 500W. The load current spectrum has negligible harmonic contents.

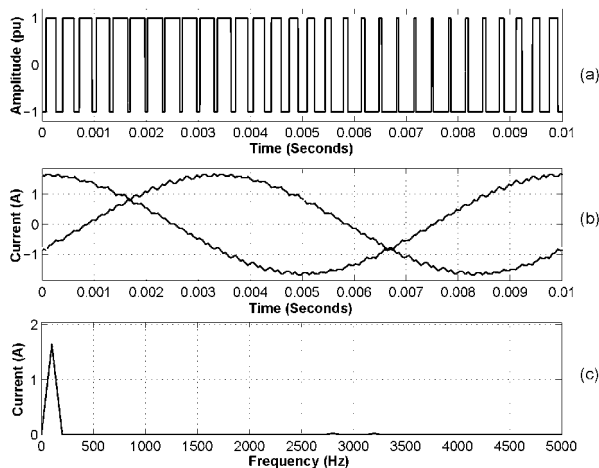


Fig. 7 Simulation results for $N = 30$, $f = 100$ Hz, $M=0.8$, motor current, $I_m = 1.7$ A, (a) PWM waveform for Q_1 switch of the inverter, (b) current waveforms for three phases, and (c) load current spectrum.

The ASD scheme is tested experimentally upto a speed of 4000 rpm and found to operate efficiently. The load current waveform is found to be in close match with the simulated waveforms. Typical experimental waveforms are shown in Fig. 8. The harmonics in current waveform are very small that proves the high performance of the scheme.

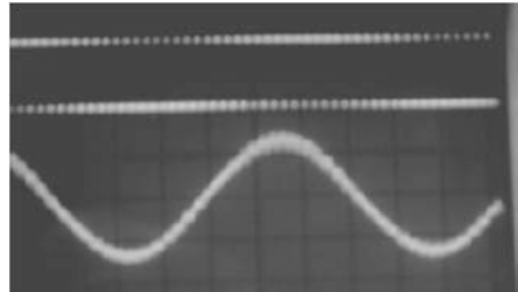


Fig. 8 Photograph of PWM switching pattern for Q_1 , and phase A current waveform at a carrier frequency of 3KHz, ($V_s = 300$ V, the load is a three phase induction motor at 500W and 1000 rpm).

6. CONCLUSION

A new concept of high resolution PWM technique for inverters of AC drives is proposed in this paper. Interruption of the processor is very small for generating such high resolution PWM. When implemented in ASD, the processor can be made engaged for computation of the proper operating frequency for its efficient operation at any operating point. A low-cost and low-speed processor is sufficient for this scheme making it feasible for commercial and household application.

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