

Karakonstantis Georgios

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Keywords: VLSI, DSP, Computer Architecture, Low power Design, Voltage Over-scaling, Process Aware Design, Digital System Design, Low Power and Robust Memory Design, ASIC, FPGAs, SoC Design.

EDUCATION

- **PhD [08/2005-present]: School of ECE, Purdue University, IN, USA**
Expected Graduation: May, 2010
Primary Research Area: VLSI and Circuit Design
Secondary Research Area: Signal & Image Processing, Nanotechnology
Research Advisor: Prof. Kaushik Roy
Thesis: “Algorithm/Architecture Co Design for Low Power and Parametric Robustness through Voltage Over-scaling, Unequal Error Protection & Quality Modulation”
Graduate Courses: Advanced VLSI Design, Digital VLSI Design, Analog VLSI Design, Solid State Devices, Digital Signal Processing, Computer Architecture, Digital Communications, Image Processing, Introduction to Optimization, Linear Algebra, Advanced Math for Engineers.
- **Diploma [07/2005]: School of Computer & Communication Engineering, University of Thessaly, Volos, Greece.**
Major: Hardware and Computer Architecture
Thesis Advisor: Prof. Georgios Stamoulis and prof.. Nikolaos Bellas (Motorolla, Inc)
Thesis: “Design and implementation of a hardware and software interface for an image sensor on a System On Chip for image processing and video compression.”

RESEARCH EXPERIENCE

- PhD Thesis, goal:** Integrated design methodology that independent of process technology results into voltage over-scalable and highly reliable systems while staying under the power/performance/quality envelope.
- **Design Methodology for the design of Low Power and Error Resilient DSP architectures**
 1. In the algorithmic level identify critical components that contribute significantly to quality
Minimize complexity by modifying less critical computations.
 2. Map modified algorithm to architecture by giving priority to more important computations.
 3. Graceful degradation of output quality under aggressive scaling of supply voltage and/or delay failures due to process variations.
 4. Trade off power, output quality and error resiliency.
 5. Application to the design of Color Interpolation Filtering, Discrete Cosine Transform (DCT) Motion Estimation (Video) and Fast Fourier Transform (under preparation).
 - **Low-Power Process-Variation Tolerant Arithmetic Units Using Input-Based Elastic Clocking**
 1. Design of low power and process tolerant adders (ripple carry, carry select) and multipliers (wallace tree, carry save). Incorporate the proposed arithmetic units in a five stage pipeline.
 2. Isolate critical paths, make them predictable and avoid the possible errors by adaptive clock stretching.
 3. Correct operation under aggressive supply scaling and/or process variations meeting target performance.

- **DSP System Level Synthesis using Unequal Error Protection and Voltage Over-Scaling (VOS)**
 1. Depending on user specifications and severity of process variations/channel noise, the degree of VOS in each block of the system is adaptively modulated to ensure minimum system power while providing “just-the-right” amount of quality and robustness
 2. Take into consideration system level interactions and ensure that under any change of operating conditions only the “less- crucial” computations, that contribute less to block/system output quality, are affected
 3. Application to the design of a DCT/IDCT System
 4. Develop the mathematical framework for the exploration of Energy-Quality efficiency of DSP Systems.
 5. Application to the design of a Low Power and Robust Memory
- **Algorithm/Architecture co-optimization for low power design**
 1. Develop an optimal algorithm based on chebychev criterion for the generation of coefficients that conform to a given low-power architecture, while meeting the given filter specifications.
 2. Use the modified coefficients for the VLSI implementation of FIR filtering.
 3. Optimal algorithm for the design of coefficients with pre determined properties

VLSI Lab, University of Thessaly

Develop components (white balance, hardware interface of image sensor) for diploma Thesis. Design of memory components for the ARM microprocessor and implementation of different digital designs on FPGA (Spartan IIE).

WORK EXPERIENCE

- **Advanced Technology Group, Qualcomm Inc., San Diego, U.S.A., 05/08-09/08**
Explored the 3d integration feasibility of logic/memory and analyzed potential sensitive gates using as test vehicle an ARM processor in 45nm technology through a Variability Aware Modeling tool (VAM) that was co-developed with IMEC (Supervisor: R. Radojic).
- **VLSI Lab, Intracom Inc., Athens, Greece, 07/03 – 09/03**
Involved in a Telecom-VLSI project. Designed and implemented the SPI-3 Interface, a protocol for the interconnection and communication of PHY-Layer and Link-Layer of a device. Worked on a FPGA system and became familiar with system-level design issues (Supervisor: D. Kritharidis).
- **Telemedicine Lab, Foundation of Technology and Research, Irakleion, Greece, 07/02 –08/02**
Design and implementation of the interface of the medicine appliance 'Spiro meter' with a computer device, funded by the European program HYGEIANet (Supervisor: K. Chronaki).
- **Computing and Network Organization (NOC), University of Thessaly, Greece, 07/01 –09/01**
Participation in the project "Iraklitos" measuring the network traffic in university's computer network and developing an environment to display network statistics (Supervisor: E. Houstis).

TEACHING EXPERIENCE

ASIC Design Lab (ECE 495d, ECE337), Purdue University, 9/05–5/07

Introduction to standard cell design of VLSI (Very Large Scale Integration) digital circuits using the VHDL hardware description language. Responsible for lecture and lab per week.

PROFESIONAL ACTIVITIES

Reviewer of IEEE Journals (TVLSI, TCAS) and IEEE conferences (ISLPED, DATE, ICECS).

PUBLICATIONS

Conferences

- C1. G. Karakonstantis**, N. Banerjee, K. Roy, C Chacrabarti, "Design Methodology to Trade-off Power, Output Quality and Error Resiliency: Application to Color Interpolation Filtering", *IEEE ICCAD*, November, 2007.
- C2. D. Mohapatra**, **G. Karakonstantis**, K. Roy, "Process Variation Tolerant Low-Power Arithmetic Units using input based adaptive clocking", *IEEE ISLPED*, August 2007.
- C3. G. Karakonstantis**, K. Roy, "An optimal algorithm for low power multiplierless FIR filter design using chebychev criterion", *IEEE ICASSP*, Page(s):II-49-II-52, April 2007.
- C4. N. Banerjee**, **G. Karakonstantis**, K. Roy, "Process Variation Tolerant Low Power DCT Architecture", *IEEE DATE 2007*, Page(s):1-6, April 2007.
- C5. G. Karakonstantis**, D. Mohapatra, K. Roy, "System Level DSP Synthesis Using Voltage Overscaling, Unequal Error Protection & Adaptive Quality Tuning: Application to DCT/IDCT," *IEEE SIPS*, 2009.
- C6. D. Mohapatra**, **G Karakonstantis**, K. Roy, "Significance. Driven Computation: A Voltage-Scalable, Variation-Aware, Quality-Tuning Motion Estimator," *IEEE ISLPED*, 2009.
- C7. G. Karakonstantis**, G. Panagopoulos, K. Roy, "A Framework for the Exploration of Energy-Quality Efficiency of Robust DSP Systems", to be submitted.

Journals

- J1. G. Karakonstantis**, N. Banerjee, and K. Roy, "Process-Variation Resilient & Voltage-Scalable DCT Architecture for Robust Low-Power Computing," to appear in *IEEE Tran. on VLSI* 2009.
- J2. N. Banerjee**, **G. Karakonstantis**, J.H. Choi, C Chacrabarti and K. Roy, "Design Methodology for Low Power Dissipation and Parametric Robustness through Output Quality Modulation: Application to Color Interpolation Filtering," to appear in *IEEE Tran. on CAD*, 2009.
- J3. S. Ghosh**, D. Mahapatra, **G. Karakonstantis**, K. Roy, "Low-power and robust circuit design under parameter variations using critical path isolation and adaptive clocking", to appear in *IEEE Trans on VLSI*, 2009.

Posters

- P1. S. Ghosh**, D. Mohapatra, **G. Karakonstantis**, K. Roy, "CRISTA: A process-tolerant, low voltage design methodology using adaptive clocking for high-performance processors", *Gigascale Systems Research Center (GSRC) Annual Symposium*, 2007.
- P2. N. Banerjee**, S. Ghosh, **G. Karakonstantis**, D. Mohapatra, J. H. Choi, K. Roy, "Yield-Centric Design Framework for Low Voltage Robust Systems", *GSRC Annual Symposium*, 2007.
- P3. G. Karakonstantis**, N. Banerjee, J. H. Choi, K. Roy, Design Paradigm for Low Power, Variation Resilient Systems using Adaptive Quality Modulation, *GSRC Annual Symposium*, 2008.
- P4. G. Karakonstantis**, K. Roy, "Algorithm/Architecture Co-Design for Low Power and Parametric Robustness through Adaptive Quality Modulation", *ACM Phd Forum, IEEE DAC*, 2009.

COURSE PROJECTS

- Implementation of high gain low power operational amplifier and active and switch capacitor filter design (Hspice).
- Implementation and performance evaluation of cache enhancement techniques in superscalar processors implemented using simplescalar (C).
- Implementation of JPEG encoder (C++).
- Pipelined FFM Multiplier (Schematic and Custom Layout Design, Hspice).
- Design and implementation of a pipelined FIR filter (Vhdl).
- Performance evaluation of image and video processing algorithms (Matlab, C).
- Implementation and evaluation of varying network topologies (simulator ns-2).
- Development of a Business plan for a Fixed Wireless Network.
- Participated and completed the project "Wireless Security" for the mapping and studying of wireless networks in the area of Volos, Greece.
- Development of an equalizer and spectrum analyzer (Java, Matlab).

TECHNICAL SKILLS

Programming Languages: *VHDL, C, Java, C++, Prolog, Visual Basic.*

Electrical S/W: *Matlab, HSpice.*

Operating Systems: *Unix, Red hat Linux, Windows XP, MS DOS, Solaris.*

Tools: *Synopsys Tools (Design Analyzer, Design Compiler, Nanosim, PowerMil, Primetime), Cadence Tools (ICFB, Virtuoso, Silicon Ensemble), Modelsim, Xilinx ISE, SimpleScalar, CPLEX, GAMS.*

Boards: Digilent Board with peripherals (Spartan IIE, FPGA), Altera DE2 Board (Cyclone II, FPGA), Digilent XUP-V2Pro Board (Virtex 2-Pro).

LANGUAGES

English (fluent, Certificate of Proficiency in English, University of Michigan Certificate, 2003),
Greek (fluent)
French (good)

SOCIETY MEMBERSHIP

- Student member of the Institute of Electrical and Electronics Engineers (IEEE)
- Student Member of the Association for Computing Machinery (ACM)
- Student member of Semiconductor Research Corporation (SRC)
- Student member of Gigascale Systems Research Center (GSRC)
- Treasurer of Hellenic Student Association, Purdue University, 2008, 2009

AWARDS

Travel Grant, Design Automation Conference (DAC), 2009.
Young Student Support, Design Automation Conference (DAC), 2007.
Distinction in Greek Parliament of Adolescents, 1999.

REFERENCES

Available Upon Request.