On The Electro-Mechanical Reliability of NEMFET as an Analog/Digital Switch

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Abstract – In this article, we identify and evaluate the major reliability issues (Negative Bias Temperature Instability, Hot Carrier Injection, and Creep) of Nano-Electro-Mechanical Field Effect Transistor (NEMFET) when used as an analog or digital switch. We use Euler-Bernoulli equation to model the static and dynamic behavior of NEMFET and couple it with classical theories of NBTI, HCI and creep to predict the associated lifetime of the device. Since NBTI and HCI are regularly observed in classical Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), we compare NBTI and HCI induced degradation in NEMFET with that of a MOSFET. We find that, NBTI time-evolution in NEMFET is comparable to that of a MOSFET. In spite of this similarity, while NBTI causes only parametric degradation in MOSFET, it changes the pull-in/pull-out voltage of NEMFET that could lead to catastrophic failure due to stiction. Next, we study HCI, which is a persistent reliability concern for MOSFET, and find that NEMFET may be immune to HCI degradation due to NEMFET’s intrinsic pull-in and release dynamics. Finally, we study time dependent mechanical creep in NEMFET for below pull-in operation and find that a time dependent increase in the off-state capacitance and power consumption may negate one of the major advantages of NEMFET as a replacement for MOSFET.

Keywords – NEMFET; Electro-Mechanical; Switch; Reliability; NBTI; HCI; Creep

I. INTRODUCTION

Nano-Electro-Mechanical Field Effect Transistor (NEMFET) is an ideal candidate for many applications such as: (i) ‘sub 60mV/decade’ switches with arbitrarily low sub-threshold slope [1, 2] because of its abrupt pull-in characteristics, (ii) a sleep transistor because of very low leakage in off-state due to the physical separation of the gate from the dielectric, (iii) resonant gate transistor [3] because of very high quality factor, etc. However, because of its relatively recent use as an analog/digital switch and radically different modes of operation, there has not been any systematic study on the reliability of NEMFET to assess its promise for becoming a viable digital/analog technology.

NEMFET is analogous to a classical MOSFET in terms of the electrical performance, except for its behavior in OFF state. Moreover, because of its superior OFF-state performance, NEMFET is considered to be a replacement for MOSFET in future [1, 2]. Therefore, many of the reliability concerns for MOSFET are also relevant for NEMFET.

For classical digital technology based on MOSFET switches, Negative Bias Temperature Instability (NBTI) [4, 5], Hot Carrier Initiated Degradation (HCI)[6], and gate dielectric breakdown (TDDB)[7] are the major reliability concerns. More recently, positive bias temperature instability (PBTI)[8] has also been considered as an important reliability concern in MOSFETs with high-κ gate dielectrics. One wonders how these reliability concerns would change if NEMFET were to replace the CMOSFET technology. Moreover, the mechanical nature of NEMFET may introduce additional reliability concerns such as creep [9], which is yet to be discussed in literature, but may have important consequences for qualification of a technology that includes sleep transistor or resonant gate transistor.

In this paper, we develop a systematic theory of electro-mechanical reliability of NEMFET related to NBTI, HCI and Creep (section II). We show that these reliability concerns have dramatically different implications for NEMFET compared to CMOS switches (section III). An intuitive understanding of these reliability issues allows us to speculate on the reliability issues such as TDDB and PBTI, etc. in the concluding section (section IV).

II. THEORY OF ELECTRO-MECHANICAL RELIABILITY OF NEMFET

a. Theory of NEMFET

The structure of NEMFET is similar to that of a MOSFET, except for the presence of a fixed-fixed beam that forms the movable gate (see Fig. 1(a)). Both the static and dynamic behavior of NEMFET is modeled by the well-known Euler-Bernoulli equation, which accounts for the bending of the beam along its length:

$$\rho W H \frac{\partial^2 y}{\partial t^2} + E I \frac{\partial^4 y}{\partial x^4} = -\frac{1}{2} \epsilon_0 E_{air}^2 W,$$  \hspace{1cm} (1)

where $\rho$ is the density, $W$ is the width, $H$ is the thickness, $y(x)$ is the deflection of a point at location $x$ on the beam, $t$ is time, $E$ is the Young’s modulus, $I = \frac{WH^3}{12}$ is the second moment of area of the beam. The right hand side in Eq. (1) is the electrostatic force per unit length acting on the beam,
where $E_{\text{air}}$ is the electric field in air, and $\epsilon_0$ is the permittivity of free space. The electric field in the air $E_{\text{air}}$ can be expressed in terms of the electric field at Si-SiO$_2$ interface and interface trap density, i.e.,

$$E_{\text{air}} = \epsilon_a E_a = \epsilon_0 E_a(\psi_s) + \frac{q N_{IT}}{\epsilon_0}, \quad (2)$$

where $\epsilon_a$ is the dielectric constant of SiO$_2$, $E_a$ is the electric field in SiO$_2$, $\epsilon_s$ is the dielectric constant of Si, $E_s(\psi_s)$ is the electric field at Si-SiO$_2$ interface, $\psi_s$ is the surface potential, $q$ is the elementary charge on electron, and $N_{IT}$ is the interface trap density at Si-SiO$_2$ interface. Now, using the Kirchhoff’s voltage law which relates the voltage drop in air, SiO$_2$ and Si with the applied gate voltage ($V_G$), we get:

$$V_G = (y(x) + \frac{y_F}{\epsilon_a}) E_{\text{air}} + \psi_s(x), \quad (3)$$

where $y(x)\epsilon_s E_s(\psi_s(x))$ is the voltage drop in air at location $x$, and $\frac{y_F}{\epsilon_a} E_s(\psi_s(x))$ is the voltage drop in the dielectric.

Equations (1)-(3) are solved self-consistently to calculate the shape of the beam $y(x)$ and surface potential $\psi_s(x)$ at any $V_G$.

The corresponding inversion charge density ($Q_i$) in the channel and drain current ($I_{DS}$) are obtained by Eqs. (4)-(6):

$$Q_i(x) = \frac{q n_i^2}{N_A} \int_0^{\psi_s(x)} \frac{q \psi}{E_s(\psi)} d\psi, \quad (4)$$

$$E_s(\psi) = \left[ \frac{2qN_A}{\epsilon_0 \epsilon_s} \right] \psi + \left( e^{\frac{q \psi}{k_B T} - 1} - 1 \right) \frac{k_B T}{q}$$

$$- \left( \frac{n_i}{N_A} \right)^2 \left( \psi - \left( e^{\frac{q \psi}{k_B T} - 1} - 1 \right) \frac{k_B T}{q} \right)^2, \quad (5)$$

$$I_{DS} = \mu \frac{V_{DS}}{W} \int_0^L Q_i(x) \, dx, \quad (6)$$

where $n_i$ is the intrinsic carrier concentration in the substrate, $N_A$ is the substrate doping concentration, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $\mu$ is the channel mobility for electrons in n-type NEMFET or holes in p-type NEMFET, $V_{DS}$ is the applied drain to source voltage, and $L$ is the length of the beam.

Figures 1(b)-(e) show the results of static and dynamic behavior of NEMFET obtained through self consistent numerical simulations of Eqs. (1)-(6). The application of gate voltage ($V_G$) bends down the beam symmetrically, as in Fig. 1(b). Such bending of the beam increases the gate capacitance and the drain current ($I_{DS}$)(see Fig. 1(d)). The steady state shape of the beam is calculated by the balance of electrostatic and restoring spring forces (i.e., by setting the time derivative Eq. (1) to zero) [10]. For $V_G > V_{PI}$, the beam gets pulled-in giving rise to sub-threshold slope of less than 60mV/decade (see Fig. 1(d)). Further increase in $V_G$ beyond $V_{PI}$ increases the contact area of the beam with the dielectric (see Fig. 1(b)) and thereby increases the capacitance. Increase in $V_G$ also increases the inversion charge in the channel. As a consequence of this increase in the inversion charge, drain current continuously increases beyond $V_{PO}$. During pull-out, $V_G$ must be reduced below $V_{PO}$ to restore the beam into its original shape. During this release phase (see Fig. 1(e)), first the contact area of the beam reduces, and then at $V_G = V_{PO}$.
the beam touches the dielectric only at a single point (see Fig. 1(c)). Finally, for $V_g < V_{pO}$, beam comes back in air. Given this basic background of pull-in and pull-out dynamics of a NEMFET, we are now ready to explore the reliability implications for NEMFET switches.

Fig. 2: Negative Bias Temperature Instability (NBTI) in NEMFET under (a) DC stress when gate has been pulled-down (b) Off state during AC stress. Gate is separated from the dielectric by an air-gap when the gate voltage is removed under AC stress.

b. Theory of NBTI

Negative Bias Temperature Instability is one of the major reliability problems in classical p-type MOSFET (PMOS) biased in inversion, i.e., when the gate is negatively biased with respect to source and drain. This phenomenon is attributed to interface defect formation ($\text{Si-H} \rightarrow \text{Si-} + \text{H}$) at the Si/SiO$_2$ interface of a PMOS transistor and is consistently modeled using the Reaction-Diffusion (R-D) framework [4, 5, 11]. During ON state (when $V_g > V_{PT}$), inversion charges (holes) populate near the Si/SiO$_2$ interface. These holes are captured by the interfacial Si-H bonds and dissociate the bond creating interface defect or dangling Si- bonds (see Fig. 2(a)). The rate of such defect generation is given by,

$$\frac{dN_{IT}}{dt} = k_f (N_0 - N_{IT}(t)) - k_r N_{IT}(t) N_H^0,$$  \hspace{1cm} (7)

where $N_0$ is the initial number of Si-H bond at Si/SiO$_2$ interface, $N_{IT}(t)$ is the fraction of these Si-H bonds broken at time $t$ due to NBTI stress, $k_f$ is the dissociation constant of Si-H bond breaking process, $k_r$ is the constant for reverse reaction, and $N_H^0$ is the concentration of H atoms at the Si/SiO$_2$ interface. The H atom released in the process can anneal the interface, according to the following diffusion equation, i.e.,

$$\frac{\partial N_X}{\partial t} = D_h \frac{\partial^2 N_X}{\partial y^2},$$ \hspace{1cm} (8)

where $N_X$ is the concentration of diffusion species, which can be both H and H$_2$ [5]. Equations (7) and (8) are solved self-consistently to calculate the concentration of interface defect $N_{IT}(t)$ as a function of stress time $t$. To study NBTI in NEMFET, we solve Eqs. (1)-(8) self-consistently and present the results in section III(a-b). Our self-consistent solution suggests that while NEMFET retains the key features of defect generation as observed in MOSFET, the implications of NBTI on the operation of NEMFET is fundamentally different than those observed for classical PMOS transistors.

c. Theory of HCI

Hot carrier injection is a persistent reliability concern for CMOS technology incorporating p- and n-type MOSFETs. HCI causes degradation of the gate dielectric near the drain side of a MOSFET (see Fig. 3(a)). According to the classical theory of HCI [6], HCI is maximized when the product of the number and the energy of the channel carriers is maximized near the drain. For long channel classical MOS transistors, it typically occurs when the gate voltage is about half the drain voltage. Below this critical bias condition (i.e., at $V_g << V_{DS}/2$), there are not enough carriers near the drain-side of the channel to do any damage, whereas at higher bias (i.e., at $V_g \gg V_{DS}/2$), the carriers near the drain are not hot enough to cause any significant degradation. During such optimal bias condition of $V_g \sim V_{DS}/2$ (see Fig. 3(a)) in a simple circuit like CMOS inverter (see Fig. 3 (b)), both n- and p-type MOSFET are on simultaneously. Therefore, simultaneous conduction of n- and p-type transistors can be used as an indicator for the presence of HCI in a CMOS technology. In section III(c), we investigate the presence of simultaneous conduction of n- and p-type NEMFETs. Our study suggests that in NEMFET circuits, both the transistors are never turned on simultaneously, and, therefore, NEMFET circuits are expected to be immune from HCI degradation.

Fig. 3: (a) Classical theory of HCI suggests oxide defect creation near the drain side of a MOSFET when gate voltage is about half the drain voltage. In simple CMOS circuits like inverter, such $V_g \sim V_{DS}/2$ occurs when both p- and n-type FETs are ON during switching of input signal. (b) Schematic of the inverter, where HCI situation is simulated during $1 \rightarrow 0$ switching of input signal.

Fig. 4: Spring-dashpot model of a viscoelastic material which is used to model creep in NEMFET.
d. Theory of Creep

Creep is a time-dependent deformation phenomenon during which a material deforms when subjected to a constant load (or stress) for a prolonged period of time [9]. The creep in RF MEMS varactors has been identified as one of the major reliability problems and has been studied using theory of viscoelasticity [12, 13]. We use the same theory of viscoelasticity to model creep behavior in NEMFET also. A viscoelastic material (fixed-fixed beam in Fig. 1(a)) can be represented as a combination of linear spring (elastic element) and a dashpot (viscous element) (see Fig. 4) [14]. The linear spring follows the Hooke’s law, \( \sigma = E \varepsilon \), where \( \sigma \) is the stress, \( \varepsilon \) is the strain, and \( E \) is the Young’s modulus; whereas the dashpot follows the Newton’s law \( \dot{\varepsilon} = \eta \frac{d\varepsilon}{dt} \), where \( \eta \) is the viscosity of the material. The elastic and viscous components experience the same strain when they are in parallel, but the total strain is the sum of the two strains when they are in series. A model of creep with multiple time constants, as shown in Fig. 4, can be defined by the following stress-strain relationships:

\[
\frac{\sigma}{E_i} = \eta_i \frac{d\varepsilon_i}{dt} + \varepsilon_i, \quad i = 2, \ldots, n, \tag{9(a)}
\]

\[
\varepsilon = \frac{\sigma}{E_1} + \sum_{i=2}^{n} \varepsilon_i, \tag{9(b)}
\]

where \( E_i \) is the Young’s modulus, \( \eta_i \) is the viscosity, \( \varepsilon_i \) is the strain of the \( i \)th branch of the model, \( \sigma \) is the total stress, and \( \varepsilon \) is the total strain.

The steady-state EB equation (i.e., Eq. (1), with time derivative set to zero) describes the steady state elastic response (\( \sigma = E\varepsilon \)) of the beam. It is, however, necessary to use a time-dependent stress-strain relationship (i.e., Eq. (9)) of viscoelastic material to model the creep behavior in MEMS type devices like varactors or NEMFET. The following generalized EB equation (Eq. (10), see [16] for detailed derivation) accounts for the ‘spring-dashpot’ response of the beam (Eq. (9))

\[
E_i \frac{\partial^4 y}{\partial x^4} = F_{\text{electrostatic}} + E_i \sum_{i=2}^{n} \varepsilon_i^m, \tag{10a}
\]

\[
\frac{F_{\text{electrostatic}}}{E_i} = \eta_i \frac{d\varepsilon_i^m}{dt} + \varepsilon_i^m, \quad i = 2, \ldots, n, \tag{10b}
\]

where \( \varepsilon_i^m \) is an intermediate strain of the beam, and \( F_{\text{electrostatic}} = -\frac{1}{2} \varepsilon_0 E_0^3 W \) is the electrostatic force per unit length acting on the beam. The results of the creep phenomena will be discussed in section III (d).

III. RESULTS AND DISCUSSIONS

In this section, we solve equations (1)-(10) self consistently to study the effect of NBTI, HCI and creep on the long term performance of NEMFET. We also perform life time projections for each reliability criteria using simulated results.

a. NBTI (DC Stress)

The operation of NEMFET is same as that of a classical MOSFET in pulled-in state (see Fig. 2(a)), because gate is in contact with the dielectric for this configuration. For simulation purposes, we consider pure SiO\(_2\) as the gate dielectric (thickness, \( y_d = 1 \text{nm} \)), and assume that NBTI is described by classical H-H\(_2\) Reaction-Diffusion (R-D) model [5] (Eqs. (7)-(8)). During the DC stress, a p-NEMFET will always be in pulled-in state (\( |V_g| > |V_{pl}| \)) as shown in Fig. 2(a) and hence dissociation of Si-H bonds will increase the dangling bond density \( N_{TB}(t) \) as \( t^n, n = 1/6 \) (Fig. 5(a)), just like a classical MOSFET [5]. Higher \( N_{TB}(t) \) will increase the electric field in air (see Eq. 2) and hence increase the electrostatic force acting on the beam, which will result in
reduction of $V_p$ and $V_{p0}$ (Fig. 5(b)). Obviously, $N_{IT}(t)$ only affects the electrostatic force acting on the beam, whereas restoring force (fourth order derivative in Eq. (1)) remains unaltered. Figure 5 (c) shows the time evolution of $\Delta V_{p0}$ for different stress voltages $V_s$. Eventually, when $\Delta V_{p0} = V_{p0}(0)$, ($V_{p0}(0)$ is the initial pull-out voltage) the beam sticks irreversibly with the dielectric (catastrophic failure due to stiction) and can not be pulled-out even at zero applied bias. This stiction is a well-known failure mechanism of RF MEMS capacitive switches due to dielectric charging [15] and unfortunately, NEMFET will not be immune to it. Using $\Delta V_{p0} = V_{p0}(0)$ as the lifetime criteria, we calculate lifetime ($t_{off}$) of NEMFET as a function of stress voltage ($V_s$) in Fig. 5(d). Lifetime decreases exponentially with $V_s$. Therefore, even though time evolution of $N_{IT}$ in MOSFET and NEMFET is same, NBTI in MOSFET remains a parametric degradation, whereas it can lead to catastrophic failure in NEMFET.

b. NBTI (AC Stress)

Next, we compare NBTI induced degradation of NEMFET and MOSFET under AC stress condition. When gate bias is removed for classical MOSFET, $N_{IT}$ relaxes due to repassivation of dangling Si bonds [4, 5]. However, in NEMFET $N_{IT}$ relaxation is much smaller compared to classical MOSFET (Fig. 6(a)), because the gate is physically separated from the dielectric in off-state of NEMFET (Fig. 2(b)), and therefore, the hydrogen trapped within the gate can not diffuse back to repassivate dangling Si bonds (Fig. 2(b)). Instead, only the residual hydrogen species contained within the thin dielectric at the moment of electrode separation contributes to $N_{IT}$ relaxation. The hydrogen contained in the movable gate is lost forever to the gate interconnect. As a result, NEMFET degrades faster than MOSFET at low frequencies (Figs. 6(b)). At high frequency ($f > 2D_{H2}/\gamma_{H2}$, where $D_{H2}$ is the diffusion coefficient of H2), NEMFET switching speed exceeds the hopping rate of H2. Therefore, the hydrogen profile becomes insensitive to repeated opening/closing of the switch at higher frequencies, and $N_{IT}$ degradation of NEMFET and MOSFET becomes indistinguishable (Figs. 6(c)). Figure 6(d) shows the AC-DC ratio as a function of frequency, which summarizes the discussions of Figs. 6(b-c).

c. HCI

As explained in section II (c), a necessary condition for HCI degradation is that both n and p MOSFETs must be turned on simultaneously during the switching transition. Figure 7 shows the inversion charge density as a function of time during the high to low transition of input signal for both MOSFET and NEMFET. Contrary to classical MOSFET, simultaneous conduction of n- and p- MOSFETs is absent in NEMFET. During the high to low transition of a complementary NEMFET, pull-in of p-NEMFET (see the pull-in dynamics of Fig. 1(e)) happens at a time later than the pull-up of n-NEMFET (see the release dynamics of Fig. 1(e)), and, therefore, it is impossible to turn on both NEMFETs

![Fig. 6: Simulation results for NBTI in NEMFET after (a) one cycle and (b) multiple cycles of low-frequency AC stress. Unlike classical MOSFET, gate is separated from the dielectric during off-state ($V_s = 0$) in NEMFET (see Fig. 2(b)), and therefore, only the hydrogen species that are trapped inside SiO$_2$ heals the broken Si-H bonds. As a result, NBTI degradation increases at low frequency in NEMFET. (c) At high frequency, when the H-diffusion time is slower than the operating frequency of the transistor, degradations in NEMFET and MOSFET become indistinguishable. (d) AC/DC ratio for NEMFET and MOSFET plotted at different frequency for fixed stress time of 100 sec.]

![Fig. 7: Comparison of HCI in MOSFET and NEMFET. (a) In MOSFET inverter, HCI occurs when both p- and n-type MOSFETs are on (section II(c)). (b) In NEMFET, during the high to low transition, n-NEMFET is pulled-out and p-NEMFET is pulled-in. However, because of their non-overlapping dynamics (see Fig. 1(e)), it is impossible to turn them on simultaneously, thereby eliminating the issue of HCI in a NEMFET circuit completely.]
simultaneously during this transition. Hence, the logic family associated with complementary NEMFET will be intrinsically immune to HCI degradation!

d. Creep

Creep will be a reliability problem in NEMFET when it is operated below pull-in as in sleep transistor, or resonant gate transistor, etc. Even at $V_G = 0$, there will be a residual force acting on the beam, because of non-zero flat-band voltage, and the beam will be deflected. This residual force will weaken the beam by creep (as in RF-MEMS varactors [12]) and the beam will continue to move down over time (see Fig. 8(a)) and will cause air-gap to decrease. As a result of this, capacitance of the device will increase (see Fig. 8(b)). Using the spring-dashpot model of creep (Eqs. 9-10) [16], which is well calibrated against experimental observations of creep in RF MEMS varactors [16], we calculate the beam shape and capacitance as a function of time (see Fig. 8(a)-(b)). This increase in the off-state capacitance of the device will lead to increase in off-state leakage over time. Eventually, the advantage of low-power consumption, which is typically tagged with NEMFET as a replacement for MOSFET, will be diminished. Therefore, creep will be parametric degradation mode for NEMFET circuits and should be accounted while designing circuits for long term operation.

IV. Conclusion

In this paper, we have combined Euler-Bernoulli equation for beam mechanics and modern theories of NBTI, HCl, and creep to establish the electro-mechanical reliability issues of NEMFET. Using our detailed numerical simulations, we establish that although NBTI dynamics for NEMFET is same as that of a classical MOSFET under DC stress, it may lead to catastrophic failure due to stiction in p-NEMFET. Moreover, for AC stress, relaxation in NEMFET is much smaller compared to MOSFET at low frequency, but at higher frequency NBTI is indistinguishable in MOSFET and NEMFET. We also find that NEMFET based logic family will be immune to reliability issues associated with HCI. And, finally creep is identified to be a reliability problem for below pull-in operation in sleep transistors and resonant gate transistors. Although we did not discuss PBTI and TDDB issues of NEMFET, the PBTI is likely to behave similar to NBTI and will lead to stiction. In addition, we anticipate TDDB characteristics will be similar for both technologies, although the surface evolution under repeated contact may damage the NEMFET oxide and localize defect generation. The techniques of soft-landing [17, 18] like in RF-MEMS switches can be used to avoid oxide degradation due to repeated impact.


