ECE595B
CMOS Analog IC Design
Fall 2007

Byunghoo Jung
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Instructor & CAD-TA

- **Instructor:** Byunghoo Jung (494-2866, jungb@prudue.edu)
  - Office hours: M W 4:20PM~5:30PM, Room 218, MSEE Bldg, or by appointment
- **CAD-TA:** TBD (Tel:?, email: ?)
  - Office hours: TBD
  - Facilitate and maintain the use of Lab design tools

Website & Text

- Class Website: http://web.ics.purdue.edu/~jungb/ECE595B_F2007.html
- Required Text: Design of Analog CMOS Integrated Circuits by Behzad Razavi (MaGraw-Hill)
- Reference: Analog Integrated Circuit Design by David Johns and Ken Martin (Wiley)
- Other references:
  - CMOS Analog Circuit Design by Philip Allen (Oxford)
  - Analysis and Design of Analog Integrated Circuits by Paul Gray (Wiley)

ABET Outcomes

A student who successfully fulfills the course requirements will have demonstrated:

- An ability to analyze bias circuit using CMOS current mirror
- An ability to design differential operational amplifier
- An ability to analyze basic gm-C filter
- Experience in oral presentation, teamwork, and document preparation for a finished design project

Grading Policy

- Same scale for graduate and undergraduate students
- Absolute and relative scale:
  - Average < 65/100: 25% A, 40%B, 25% C, 10% D/F
  - Average > 65/100: 35% A, 40% B, 20% C, 5% D/F
  - Average > 75/100: 40% A, 45% B, 15% C
  - The final grade distribution will be adjusted based on the average and standard deviation.
- 2 mid-terms each accounting for 25% of the grade (25% x 2 = 50%)
- Design Project accounts for 40% of the grade
- Homework assignments and Quiz account for 10%
- Late projects or assignments will NOT be accepted
  - You may request extension for homework assignment or make-up exam for documented emergencies (e.g. hospitalization, death of family member, etc.) It has to be requested only BEFORE its due date.
- Any form of cheating will be reported to the Dean of students AND result in a failing grade
- Must fulfill ABET requirements to get a passing grade

Important Deadline & Exam Schedule

- Project Proposal Due: submit to the instructor (MSEE218) by 6:00PM on Sept. 14 (Fri)
- First Exam: Oct. 12 (Fri) In class exam, close book, close notebook, single side Letter paper with equations, engineering calculator
- Interim Project Report Due: submit to the instructor (MSEE218) by 6:00PM on Oct. 19 (Fri)
- Second Exam: Nov. 23 (Fri) In class exam, open book, open notebook, single side Letter paper with equations, engineering calculator
- Project Report Due: submit to the instructor (MSEE218) by 6:00PM on Dec. 12 (Wed)
- Submit homework and project reports to Instructor: *E-mail submission is accepted and encouraged.* PDF or MS-Word format only!
  - Email title AND file name:
    - ECE595B-Homework#-$-xxxxx
    - ECE595B-Project-Proposal-$-xxxxx
    - ECE595B-Project-Interim-$-xxxxx
    - ECE595B-Project-Final-$-xxxxx
    - Where # is the assignment number, $ is your first name initial, and xxxxx is your last name.

CAD Lab

- VLSI CAD Lab located in 360 Potter Engineering Center
- Solaris / Linux workstations running Cadence
- Courtesy key for after-hour access can be obtained from front desk in Potter Engineering Library
- Additional workstations in MSEE 189
- Lab orientation will be held during the second week

Collaborations & Academic Honesty Policy

- Limited collaboration among students on the design project and homework problems is encouraged
  - Verbal discussion of problems
  - Use of scratch paper or writing boards to discuss concepts and approaches to solving specific problems
  - OK to verbally compare the final answers obtained for a given problem as a method of checking their work
  - However, if you collaborate with others, please list the names of all those with whom you collaborated at the top of each solution set you hand in

Academic Honesty

- The following academic honesty rules should be considered in force at all times:
  - Never show any draft of a homework solution to another student in the class until after the homework due date and time
  - Never look at any draft of another person's homework solution until after the homework due date and time
  - Never use another person's simulation files or supply your simulation files to another person for design project and homework
  - If violated, the student will receive a failing grade and the incident will be reported to the dean of the student for further administrative action

Course Outlines: 16 weeks

1. Device physics, modeling, and layout
2. Biasing
3. Biasing
4. Single stage amplifier
5. Single stage amplifier
6. Differential amplifier
7. Differential amplifier
8. Frequency analysis. *1st Exam*
9. Frequency analysis
10. Noise analysis
11. Noise analysis
12. Feedback
13. Feedback
14. Operational amplifier. *2nd Exam*
15. Integrated filter design
16. Integrated filter design

Course Outlines

- Many equations
- Instructor will focus on the physical meanings and concepts behind the equations
- Students are expected to derive the equations

Design Project

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- Project Report Due: submit to the instructor (MSEE218) by 6:00PM on Dec. 12 (Wed)
- Submit homework and project reports to Instructor: *E-mail submission is accepted and encouraged.* PDF or MS-Word format only!
  - Email title AND file name:
    - ECE595B-Project-Proposal-$-xxxxx
    - ECE595B-Project-Interim-$-xxxxx
    - ECE595B-Project-Final-$-xxxxx
    - Where # is the assignment number, $ is your first name initial, and xxxxx is your last name.

Design Ideas

- (A) Ultra low power operational amplifier with high slew rate capability. Design an opamp that consumes low power under normal conditions but can provide large current into the load when slewing. Hint: this has to be an adaptive circuit. Static power in the nanoampere region.
- (B) A fixed gain (maybe 10) instrumentation amplifier. Gain must be very predictable. Instrumentation amplifier requires high input impedance, large input voltage swing, low noise, etc.
- (C) Folded cascade amplifier with lager gain and bandwidth (100dB gain & 1GHz BW)
- (D) Ultra low-noise low frequency CMOS opamp (Chopper stabilized, correlated double sampled or continuous time auto-zero)
- (E) One of your own

Project: Step 1 of 6

- Select project:
  - You are expected to work on a single project
  - You are advised to start thinking of topics for your final project immediately
  - All students have to design an op-amp as their first project
  - Have to complete circuit design (layout and post layout simulation is recommended but not mandatory)
  - Complete your op-amp design by the time the interim project report is due
  - You will be given more credit for innovation

Project: Still Step 1 of 6

- Select project:
  - The second part of your project will be to use your op-amp in a more complete design
  - Recommended designs are;
    - First order active RC filter AND switched capacitor filter
  - In the second part, you can work in group of two
    - If you decide to work in group of two, you have to design “second” order active RC filter AND switched capacitor filter
  - If you are selecting d) or one of your own, make sure that you check with me before you start
  - I want you to start thinking at this time and I want you to choose a general direction immediately
  - You can provide me with more completed details for the second part of the project during the interim project report

Project: Step 2 of 6

- Choose specs for the project
- Ex) If you are going to be working on a low-power opamp, choose the value of the bias current goal that you want to design for
- Performance specifications are correlated, you need to select the complete set of specifications
- You need to look at past examples (papers, books, and website) (Analog Device, TI, Linear Tech, National Semi)
- By Sept. 14, please complete a short report of what you plan to do and the performance specifications that you plan to meet
  - Where/how you think your circuit or tool will be used
  - Particulars of the most important references (pages from books and papers or website)
  - Need to be typed. Handwritten work will not be acceptable.
  - Be a little aggressive about the specifications that you select
  - It is possible that you may not be able to meet these specifications in the final design. If so, include an explanation in your final report
- Performance specifications for the op-amp you want to include are;
  - Voltage gain
  - Unity gain bandwidth
  - Phase margin
  - Slew-rate
  - Load capacitance or Load resistance (if driving off-chip loads)
  - Power and Supply voltage (0~2.5, -1.25~+1.25, 0~2, 0~1)
  - Input and output common-mode voltage
  - Offset voltage
  - Total noise
  - Optimization criteria (what you want to minimize, i.e., power, area, noise, etc)
- Project proposal: A short (3~5 pages including 1 page of cover sheet) proposal describing what you want to do in the project. I want to see a list of references, ideas, circuit concepts, etc. *15% of Design Project.*

Project: Step 3 of 6

- Complete the first part of your project
- Take the time to analyze your circuit
- Perform hand calculations and confirm using circuit simulation
- If questioned you need to be able to defend your choices
- You need to understand how the circuit works
- Analog circuit design cannot be learned by just taking lectures and tests. You have to DO IT to learn it.
- I expect a complete design; simulations to confirm your design.
- Corner simulations and Monte Carlo simulations are not required, but make sure you understand the impact of temperature / process variations, and power supply variations on your design.

Don't be a spice monkey!

Enjoy the beauty of "handcraft" design!

Project: Step 4 of 6

- Write your interim project report
  - About 10 pages
  - Needs to be neat and typed
  - Hand written reports will not be accepted
  - Even the best project if not presented well will loose its glamour
  - *30% of Design Project*

Project: Step 5 of 6

- Complete your final project
- Same as before but now you have to use your op-amp in a complete system
- Recommended
  - 1st order active RC filter and switched capacitor filter
  - 2nd order active RC filter and switched capacitor filter (if you work in group of two)
- Again hand crafted equations, completed design, and simulation results are required

Project: Step 6 of 6

- Write your final project report
- As with the interim project report, do a good job at writing
- Include everything you did on your op-amp (i.e. interim project report) in the final report
- Expect length of about 20 pages
- *55% of Design Project*

- Questions?

Quiz

1. Output impedance of ideal I source?
2. Output impedance of ideal V source?
3. Which element(s) generate noise?
   R L C Diode Transistor
4. Capacitor generates kT/C noise. Y/N
5. It is possible to build a V or I amplifier using only passive elements. Y/N
6. Noise bandwidth is always bigger than the signal bandwidth. Y/N/Never heard NBW
7. There is a system that can improve SNR, i.e., SNR(out) > SNR(in). Y/N
8. When we mention impedance matching, it means optimal power matching. Y/N
9. In cascaded system, the total gain is the “multiplication” of each stage gain. Y/N
10. In cascaded system, the total BW is same to the BW of the stage that has the minimum BW. Y/N
11. List name of noises that you know. Ex) thermal noise

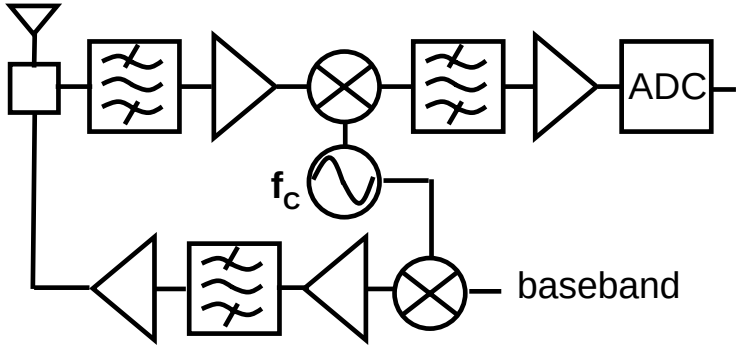
- Why analog?

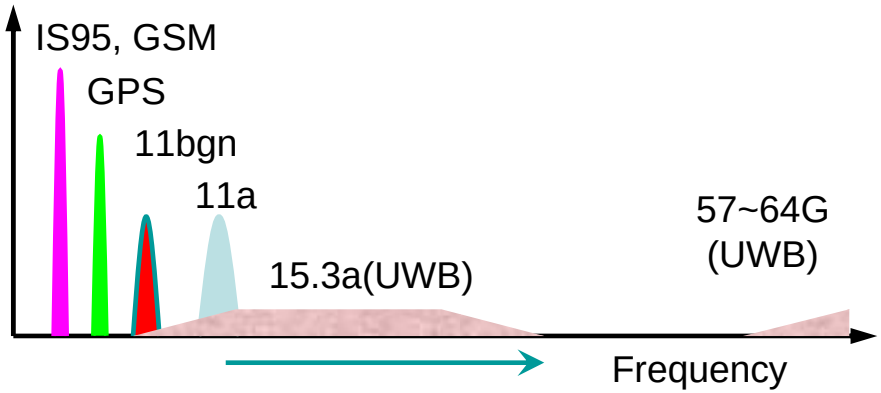
Analog Applications

- Sensor interface (P, Temp, accel, mass, gas, virus……)
- Bio system
- Audio/video applications
- Digital storage media
  - HDD CD DVD BlueRay Flash etc
  - USB, 1394
  - Read/write channel
- Every digital system with high CK speed
- RF system

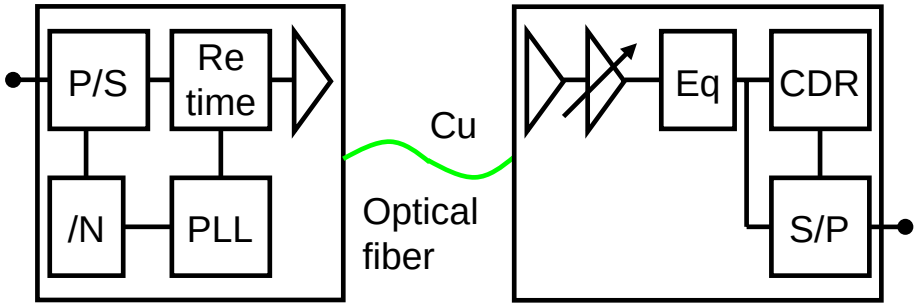
Analog Applications

- High-speed analog IC applications
  - Wireless digital communications





  - Wireline digital communications

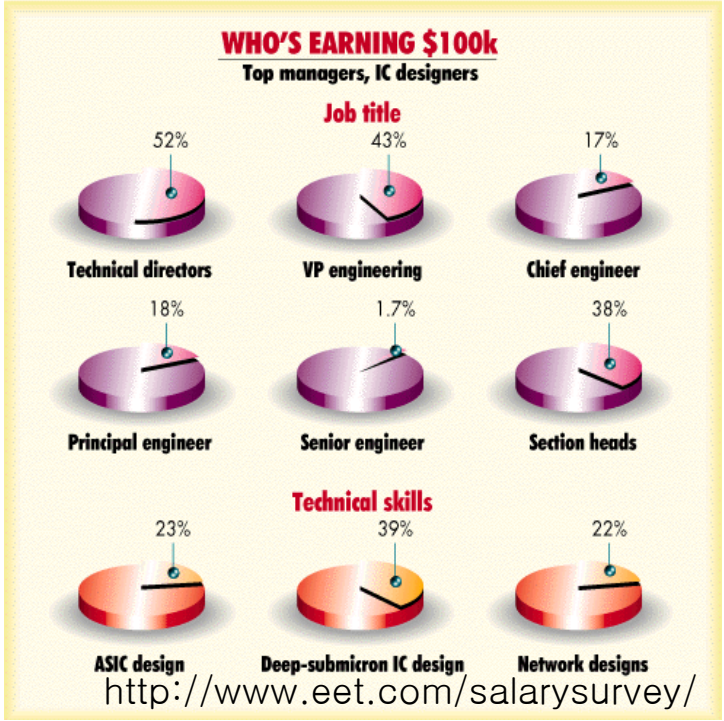


PCI Express 2.0	533MTps(4.3Gbps)
Hyper Transport 2.0	2.8GTps(22.4Gbps)
SONET (OC768)	40Gb/s
InfiniBand	100Gb/s
Chip to chip	~Tbps

Has the analog job market emerged into daylight? Certainly brighter times are upon us

http://www.planetanalog.com/showArticle.jhtml?articleID=16401444

- By Gary Fowler, President and CEO, Career Analog. Inc. PlanetAnalog December 2, 2003 (8:39 PM EST)
- Consequently, we're seeing analog job requisitions in several key areas including WiFi (wireless LANs and Internet access), ultra wideband technology (UWB) and power management. Demand for designers with expertise in high-speed data conversion seems to be high across a variety of industries.
- At the height of communications funding bubble, designers of Serdes, CDR (clock-data recovery) and PLL (phase-locked loops) could count on receiving 10 job offers almost as soon as they flashed their resumes. While the comms bubble has burst, there remain a number of openings for designers with solid analog experience.



http://www.eet.com/salarysurvey/

- Are brains analog, or digital?
- Hell breaks loose after Cornell claim
- By Andrew Orlowski in San Francisco
- Published Saturday 2nd July 2005 11:10 GMT
- A new study conducted at Cornell University suggests that we think in analog, not digital. It's a bold claim which, if true, threatens to make thirty years of linguistics and neuroscience metaphors look very silly indeed.
- Professor Michael Spivey, a psycholinguist and associate professor of psychology at Cornell claims that the mind "should be thought of more as working the way biological organisms do: as a dynamic continuum, cascading through shades of grey."

- It's bad enough that hundreds of people are already "designing" CMOS VLSI without any significant knowledge of silicon devices and circuits and sometimes without much idea of the physics of hardware in the broader sense. As electronic systems become increasingly complex, this type of design will inevitably dominate, certainly for large-scale digital systems. But I wonder how many potentially useful ideas in the meadowlands of analog circuits will never be discovered because the world of the twenty-first century was taught that analog is dead? Barrie Gilbert, "Where do little circuits come from?"
- As an old analog guru once said when comparing the analog and digital disciplines, "Any idiot can count to one, but analog design requires the engineer to make intelligent trade-offs to optimize a circuit." Analog design is not black or white as in "ones" and "zeros;" analog design is shades of gray. Samual Wilensky, "Reflections of a dinosaur"

- All the world is an analog stage and digital circuits play only bit parts. Anonymous
- *Analog circuit design is like chess–just because you know how the pieces move doesn't mean you know how to play the game. Patrick M. Lahey*

- Some twenty years ago, I asserted at a seminar presented at UC Berkeley that the art of analog design demanded 30% attention to the signal path and 70% to biasing. The comment was met with tolerant disbelief. However, after having taught this maxim widely and peresistently during the intervening decades, I find no reason to change my mind.
- — BARRIE GILBERT, “Biasing Techniques for RF/IF Signal Processing