# ECE 595B CMOS Analog IC Design (3cr), Fall 2007

**Class Schedule:** MWF 3:30PM ~ 4:20PM, EE 115

**Prerequisite:**

- ✓ ECE 255 Introduction to Electronic Analysis and Design
- ✓ ECE 455 Integrated Circuit Engineering for undergraduate students or Permission of Instructor

**Instructor:** Byunghoo Jung (494-2866, jungb@prudue.edu)

Office hours: MW 4:20PM~5:30PM, Room 218, MSEE Bldg, or by appointment

**CAD-TA:** TBD (?, ?), Office hours: TBD

Facilitate and maintain the use of Lab design tools

**Class Website:** http://web.ics.purdue.edu/~jungb/ECE595B_F2007.html

**Required Text:** Design of Analog CMOS Integrated Circuits by Behzad Razavi (MaGraw-Hill)

**References:** Analog Integrated Circuit Design by David Johns and Ken Martin (Wiley)

**Course Outcomes (ABET):**

A student who successfully fulfills the course requirements will have demonstrated:

- ✓ An ability to analyze bias circuit using CMOS current mirror
- ✓ An ability to design differential operational amplifier
- ✓ An ability to analyze basic gm-C filter
- ✓ Experience in oral presentation, teamwork, and document preparation for a finished design project

**Exam and Design Project Schedule**

- ✓ **Project Proposal Due:** submit to the instructor (MSEE218) by 6:00PM on Sept. 14 (Fri)
- ✓ **First Exam**: Oct. 12 (Fri) In class exam, close book, close notebook, single side Letter paper with equations
- ✓ **Interim Project Report Due:** submit to the instructor (MSEE218) by 6:00PM on Oct. 19 (Fri)
- ✓ **Second Exam**: Nov. 23 (Fri) In class exam, open book, open notebook
- ✓ **Project Report Due:** submit to the instructor (MSEE218) by 6:00PM on Dec. 12 (Wed)
- ✓ **Submit homework and project reports to Instructor:** E-mail submission is accepted and encouraged. PDF or MS-Word format only!

**Grading Policy**

- ✓ Same scale for graduate and undergraduate students
- ✓ Absolute and relative scale:
  - ➢ When the average is lower than 65/100: 25% A, 40%B, 25% C, 10% D/F
  - ➢ When the average is over 65/100: 35% A, 40% B, 20% C, 5% D/F
  - ➢ When the average is over 75/100: 40% A, 40% B, 20% C
  - ➢ The final grade distribution will be adjusted based on the average and standard deviation.
- ✓ 2 mid-terms each accounting for 25% of the grade (25% × 2 = 50%)
- ✓ Design Project accounts for 40% of the grade
- ✓ Homework assignments and Quiz account for 10%
- ✓ Late projects or assignments will **NOT** be accepted
  - ➢ You may request extension for homework assignment or make-up exam for documented emergencies (e.g. hospitalization, death of family member, etc.) It has to be requested only BEFORE its due date.
- ✓ Any form of cheating will be reported to the Dean of students AND result in a failing grade

- ✓ Must fulfill ABET requirements to get a passing grade

**CAD LAB**

- ✓ VLSI CAD Lab located in 360 Potter Engineering Center
- ✓ SUN workstations running Cadence and HSpice
- ✓ Courtesy key for after-hour access can be obtained from front desk in Potter Engineering Library
- ✓ Additional workstations in MSEE 189
- ✓ Lab orientation will be held during the second week

**Course Design Project**

Please refer PROJECTS guidelines.

**Collaboration and Academic Honesty Policy**

Limited collaboration among students on the design project and homework problems is encouraged. Such collaboration may include verbal discussion of problems, and the use of scratch paper or writing boards to discuss concepts and approaches to solving specific problems. It is also OK for students to verbally compare the final answers obtained for a given problem as a method of checking their work. However, if you collaborate with others, please list the names of all those with whom you collaborated at the top of each solution set you hand in.

**The following academic honesty rules should be considered in force at all times:**

- ✓ Never show any draft of a homework solution to another student in the class until after the homework due date and after that person has handed in his/her own solution set.
- ✓ Never look at any draft of another person's homework solution until after the homework due date and after you have handed in your solution set.
- ✓ Never use another person's simulation files or supply your simulation files to another person for design project.

If any of the above academic honesty rules are violated by any student in the course, the student will receive a failing grade for the course and the incident will be reported to the dean of the student for further administrative action.

**Course Outline: 16 weeks**

1. Device physics, modeling, and layout
2. Biasing
3. Biasing
4. Single stage amplifier
5. Single stage amplifier
6. Differential amplifier
7. Differential amplifier
8. Frequency analysis. 1st Exam
9. Frequency analysis
10. Noise analysis
11. Noise analysis
12. Feedback
13. Feedback
14. Operational amplifier. 2nd Exam
15. Integrated filter design
16. Integrated filter design