On-chip silicon based waveguide with light guiding in low index core materials

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ABSTRACT: A new on-chip silicon-based Bragg cladding waveguide with full CMOS compatibility is developed. This novel optical waveguide has a low refractive index core (SiO_2) surrounded by a 1D photonic crystal cladding. The cladding consists of several dielectric bilayers, where each bilayer consists of a high index-contrast pair of layers of Si and Si_3N_4. This new waveguide guides light based on omnidirectional reflection, reflecting light at any angle or polarization back into the core. Its fabrication is fully compatible with current microelectronics processes. In principle, a core of any low-index material can be realized with our novel structure, including air. Potential applications include tight turning radii, high power transmission, nonlinear properties engineering and biomaterials sensors on silicon chip.

Recently, interest in guiding light within low-index materials (including air) has increased, with new devices that use a photonic band gap (PBG) [1-3] or Bragg reflection [4-8] to confine light. Specific examples include 2D photonic crystal fibers [9-11] and ARROW waveguides [12]. Another example, the omniguide fiber, uses high index contrast concentric dielectric layers to enhance the mode confinement in a relatively simple structure [13-17]. It is difficult to fabricate this structure on a silicon chip. However, the same principle of using 1D omnidirectional mirrors can be applied to an alternative structure that can be fabricated with current microelectronics technology processes (CMOS compatible processes). Toward that end, an on-chip silicon-based Photonic Crystal (PC) cladded waveguide is designed with low refractive index material for the core, and stratified high index contrast dielectric layers as the cladding. Due to the high index contrast of these materials with each other, they have a large photonic band gap, and may act as omnidirectional reflectors, which means light of all incident angles and polarizations is reflected within a range of wavelengths (e.g., near 1550 nm). In contrast with an index-guided waveguide, it is possible to confine light to a low index core (possibly air). The high index contrast allows the cladding thickness to be less than 2 microns, which is much thinner than the conventional silica optical bench waveguide. This structure can also be used to efficiently transmit light about bends much tighter than found in low index contrast index-guided waveguides [18].

The on-chip PC waveguide is designed with a low index core layer of SiO_2 (n=1.46) and a high index contrast cladding consisting of pairs of layers of Si (n=3.5) and Si_3N_4 (n=2.0), which each have a quarter wavelength thickness at the target wavelength of 1550 nm. The on-chip PC cladded waveguide configuration is illustrated in Fig. 1. It combines the ease of layer-by-layer fabrication (as discussed below) with low losses that are associated with the presence of a highly reflective mirror on all sides of the core. Guided modes can be found within the PBG of the 1D Si/Si_3N_4 PC. They can be predicted by comparison with a waveguide made from perfectly reflecting metallic walls. The dispersion (relation between frequency and axial wavevector) for modes within the band gap of an on-chip PBG waveguide for a core size of 2.5

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microns square is shown in Fig. 2. The dispersion of the dielectric waveguide matches pretty well with the metallic waveguide, except for one key difference, which is the phase shift associated with reflections from the dielectric surface. For a perfect metal, the phase shift will always be π, but for a dielectric reflector, it will change with frequency, and generally be less than π for the lower half of the gap and greater than π for the upper half of the gap. Qualitatively, that leads us to predict that modes for the metallic waveguide are "pushed" toward the center of the gap. Another consideration is power loss in this structure. Losses will decrease with increasing core size according to a power law, and decrease exponentially with the number of cladding layers (until other loss mechanisms begin to dominate). Based on theoretical considerations, it seems that the TE_{01} mode should be capable of achieving especially low losses due to its insensitivity to core size in one direction (which allows for the lowest loss in a given modal area).

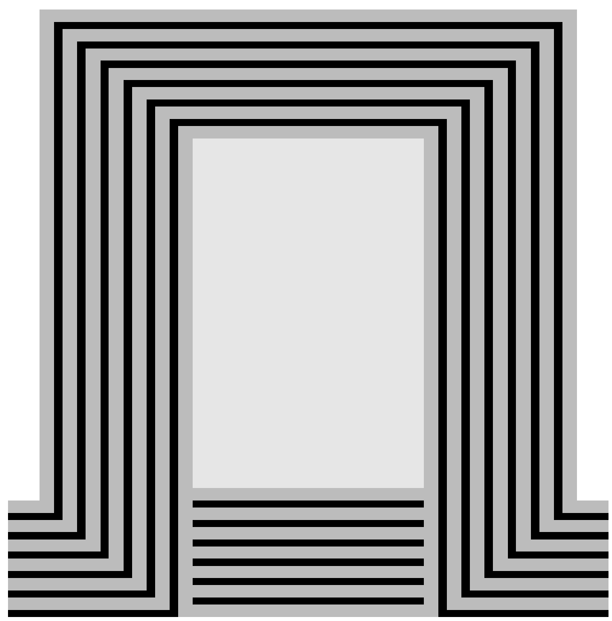


Fig.1 The illustration of the Photonic Crystal (PC) cladded waveguide, with low index core (SiO_2) and Si/Si_3N_4 as dielectric cladding layers.

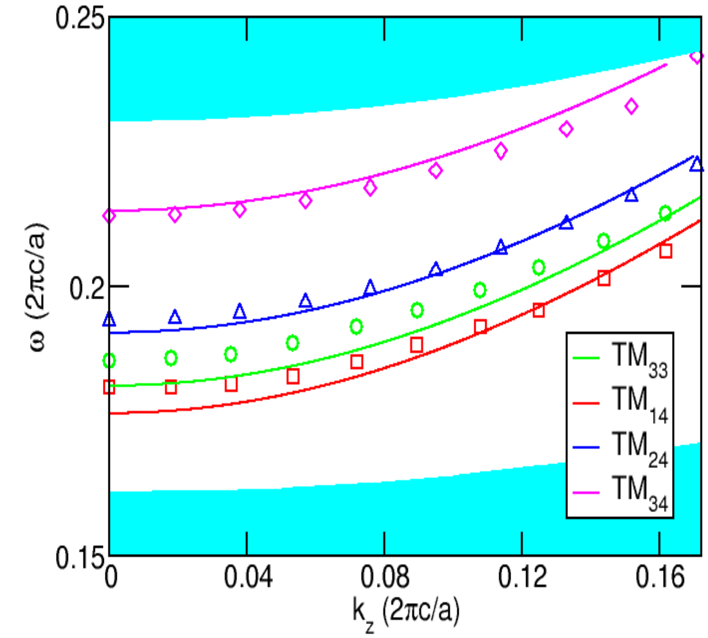
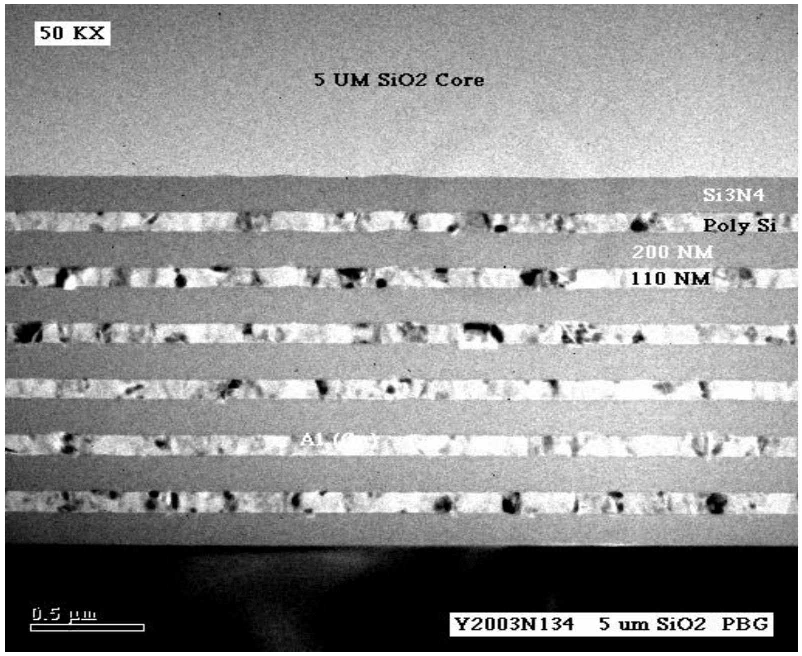


Fig.2 Dispersion relation for modes within the band gap of an on-chip PC cladded waveguide with a core of size *8a* by *8a* (*a* is the unit length of the cladding), n_{core} = 1.46, numerical data (dotted lines) from time domain calculations at specific k_z values are compared to the metallic waveguide (solid lines). TE modes are nearly degenerate with TM modes.

The on-chip PC waveguide is fabricated with a CMOS-compatible process: the Low Pressure Chemical Vapor Deposition (LPCVD) is used to deposit the Si and Si_3N_4 cladding layers and the Low Temperature Oxide (LTO) method is used to make the oxide core. On a 6" Si chip, the 110 nm Si layer is deposited using the LPCVD method at a temperature of 625°C; the 194 nm Si_3N_4 layer is deposited using LPCVD at a temperature of 775°C. After the deposition of the bottom six and a half 1D PBG crystal layers, we use the LTO method to deposit SiO_2 at 450°C, followed by a 900°C anneal, to obtain a high quality oxide layer with a thickness between 4 and 6 microns. Lithography and high-density plasma etching is then used to define the waveguide core geometry. Finally, the same deposition method (LPCVD) is used to finish the top six and a half Si/Si3N4 1D PC layers. Fig. 3a is a TEM picture of a 1D PC slab fabricated using this technique, consisting of 7 layers of Si_3N_4 and 6 layers of poly-Si arranged in a periodic structure, with top SiO_2 layer and on Si substrate. Clearly, the LPCVD deposition method is able to accurately control the thickness and flatness of the Si and Si_3N_4 layers, both of which are important to prevent scattering losses. The high index contrast of the Si and Si_3N_4 pairs gives rise to a large PBG and high reflectivity (greater than 99%) for only a few bilayers. This is illustrated in Fig.3b, where the measured absolute reflectivity of five Si/Si_3N_4 bilayers is compared with a numerical calculation of the reflectivity of the ideal structure, using the transfer matrix method. The measurement and calculation are in very good agreement with each other, most importantly in the stop band, which extends from 1200nm to 2000nm.

(a)



(b)

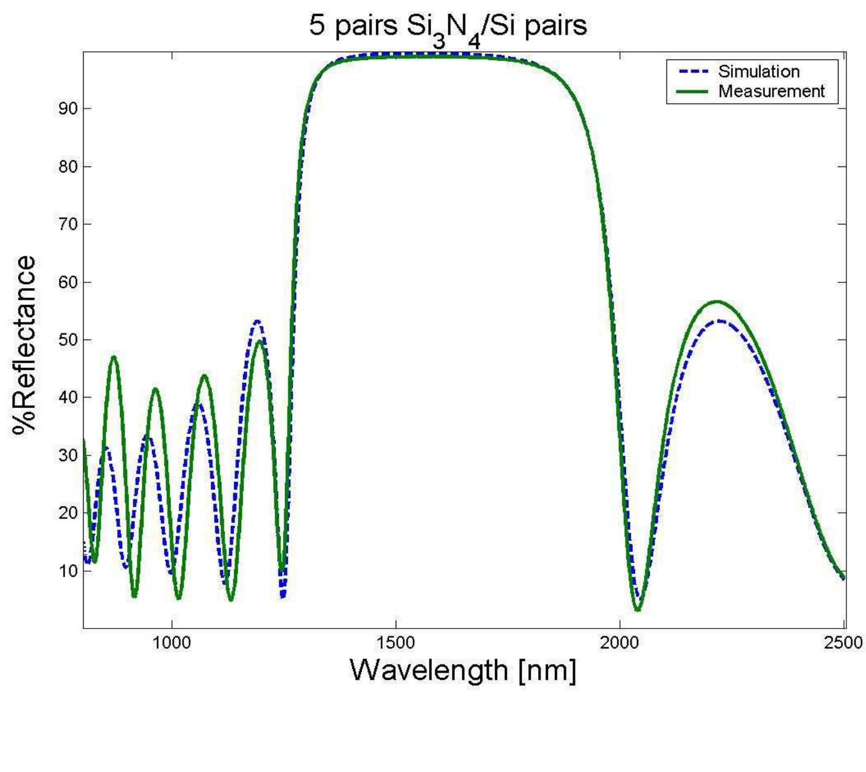
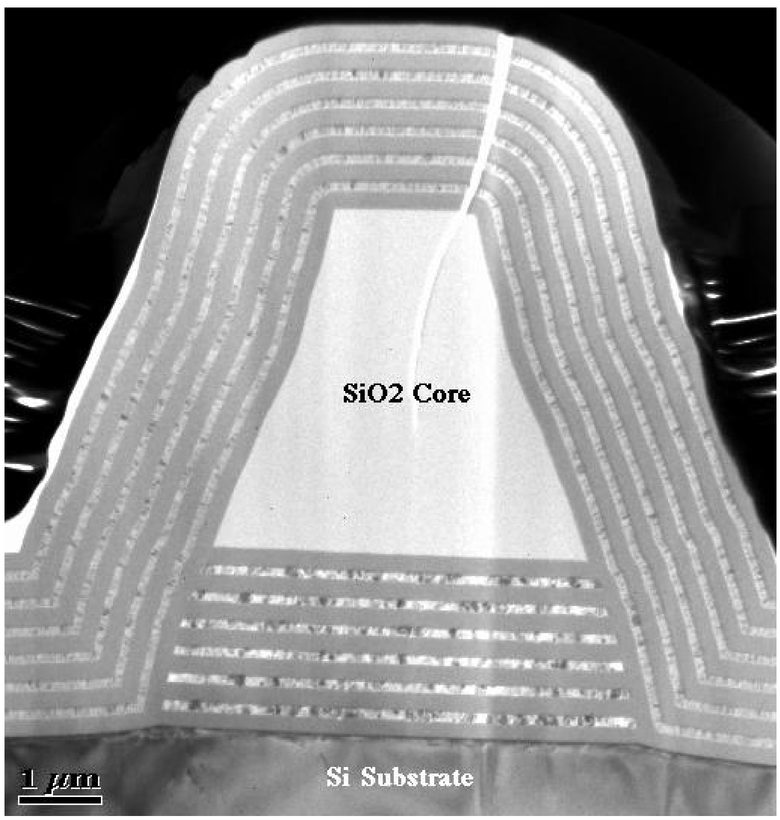


Fig.3 (a) The TEM image of the cladding pairs including the bottom cladding PBG layers (Si/Si_3N_4) and SiO_2 core. (b) The measurement and simulation on absolute reflectivity of 5 pairs Si/Si_3N_4 layers.

A TEM picture of the final product, the fabricated on-chip PC waveguide, is shown in Fig. 4a. For the top PC cladding layers, each individual Si and Si_3N_4 layer is smooth, even at the curved surface, which shows the high quality of LPCVD's conformal step coverage. From Fig. 4a, we conclude that CMOS compatible high and low index materials have good thermal and mechanical properties. The on-chip PC cladded waveguide loss is measured at 1550nm using the following procedure: light from a tapered optical fiber is coupled into the waveguide, then the guided light emerging from the other end is focused with a lens and collected with a camera. Fig. 4b shows the guided spot imaged by the camera, which demonstrates the presence of one or more well-defined guided modes, which are primarily concentrated in the low index SiO_2 core, the waveguide loss is as low as 4 dB/cm for a typical cross section 6μmx12μm.

(a)



(b)

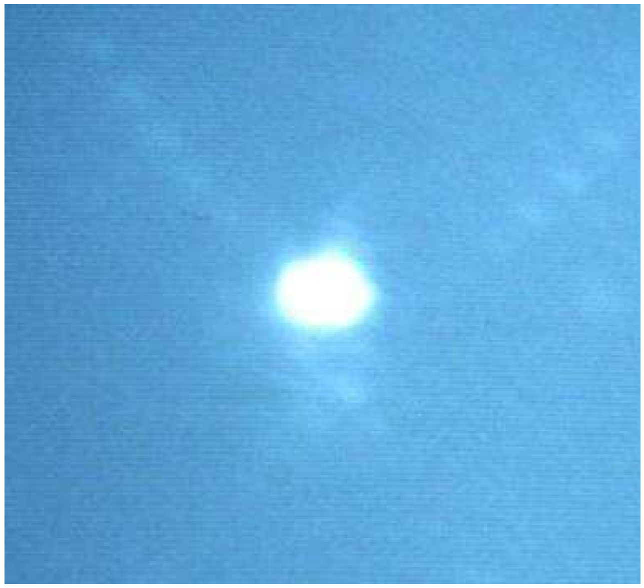


Fig.4 (a) The TEM image of the fabricated PC cladded channel waveguide. The smooth interface and good conformal step coverage by LPCVD method are clearly seen. (b) The guided spot from the PC cladded channel waveguide with dimension 4μmx4μm, which demonstrated the guidance in the low index SiO_2 materials by PBG guiding mechanism.

In this work, a SiO_2 core is used in the example of on-chip PC cladded waveguide structure. However, fabrication need not be restricted to SiO_2 – a hollow core could also be fabricated with a slight change in the procedure. This so-called "core freedom" would give rise to multiple applications, for example, transmission of high intensity beams (e.g., for a CO_2 laser) through a hollow core without absorption or nonlinearity, or to trap light -- or even modify the rate of emission -- from an optically active material. It also has unique group-velocity dispersion characteristics, which can be modified with changes to the core. Finally, the on-chip PC cladded waveguide has the advantage of relatively small dimensions, including a tight turning radius compared to low-contrast index-guided fibers. This will be explored more fully in a future work [18].

In conclusion, a new photonic crystal cladded waveguide, whose fabrication is fully compatible to the current CMOS technology, is developed. Si and Si_3N_4 are deposited using LPCVD method and high quality PC cladding layers are realized. Light guiding in the low index core is demonstrated. A thin PBG cladding, made possible by the large index contrast between the Si and Si_3N_4 layers, indicates the advantage of this device over traditional silica optical bench waveguides.

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