

MECHANISM OF DRAIN DISTURB IN SONOS FLASH EEPROMS

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ABSTRACT

We investigate the mechanism of drain disturb in SONOS flash memory cells. Our results show that drain disturb can be a serious concern in programmed state and is caused by injection of holes from substrate into the nitride. We identify the key factors responsible for this to be band-to-band tunneling at the drain junction and impact ionization of the channel leakage current. [Keywords: SONOS EEPROMs, Drain Disturb, BTBT, Charge Pumping]

INTRODUCTION

SONOS Flash EEPROMs have generated much interest in recent times due to their ease of integration into embedded systems and multi-bit storage capability via spatial localization of trapped charges [1-3]. However they also have serious reliability problems, among which endurance and data retention have received much attention [3-6]. This work shows that program drain disturb also poses a serious problem and must be considered for reliable design of memory cell.

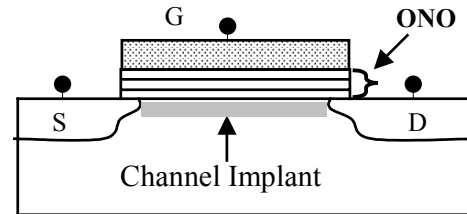
Drain disturb (or drain stress) occurs in those cells of a NOR flash array that share the bit line of the cell being written by hot-carrier injection [7]. Unlike conventional floating gate cells that show both charge gain and charge loss disturb [8], it is seen that SONOS cells mainly suffer charge loss disturb from the programmed state. While the end result is similar to charge loss during retention (caused by the redistribution and decay of charges in ONO stack [4-6]), it is shown that drain disturb involves hole injection from Si substrate into the ONO stack. The mechanism of drain disturb is established and its dependence on cell doping and bias is discussed here.

EXPERIMENTAL DETAILS

All the measurements were done on stack-gate SONOS cells with ONO thickness of 5.8/8/5 nm, width of 2 μm and drawn gate lengths (L) 0.25 and 0.35 μm . Three doping schemes were used – with and without channel compensation and halo implants – as shown in Fig. 1. Most of the results shown are from non-compensated, no-halo cells unless specifically mentioned otherwise.

Program and Erase were done using channel hot electron injection and band-to-band tunneling (BTBT) induced hot hole injection, respectively. During drain disturb measurements, gate terminal was grounded and other terminals had the same bias as in program. Disturb measurements in programmed cells were done after programming a virgin cell for a threshold voltage (V_{TH}) shift of 2 V. V_{TH} was measured from the $I_{\text{D}}-V_{\text{G}}$ using constant current method (at $V_{\text{D}} = 0.1\text{V}$). $I_{\text{D}}-V_{\text{G}}$ measurements were done in reverse read mode by interchanging source and drain terminals during read [1]. Charge pumping measurements were done at a frequency of 400 kHz using variable- V_{TOP} and variable- V_{BASE} methods [9]. For the gate induced drain leakage (GIDL) measurements V_{D} was fixed at 2 V and V_{G} was varied. $I_{\text{D}}-V_{\text{G}}$ measurements were done at periodic (logarithmic)

time intervals during program, erase and disturb, whereas CP and GIDL measurements were done at the start and at the end.



Device	Channel Implant	Natural V_{TH} (V)
Non-compensated	B	2.5
Compensated	B, BF_2 , As	0.9
Non-compensated, halo	B	3.2

FIGURE 1. SCHEMATIC AND DOPING DETAILS OF THE SONOS CELLS USED FOR MEASUREMENTS.

RESULTS AND DISCUSSION

Fig. 2 shows the change in V_{TH} with time during program, erase and drain disturb in programmed state. The drain disturb in erased state was found to be negligible in the above time scale and is not shown here. During disturb, charge loss from the programmed state is clearly observed. This could be due to escape of electrons from the ONO stack (retention issue) or injection of holes into it (soft erase), which is clarified next.

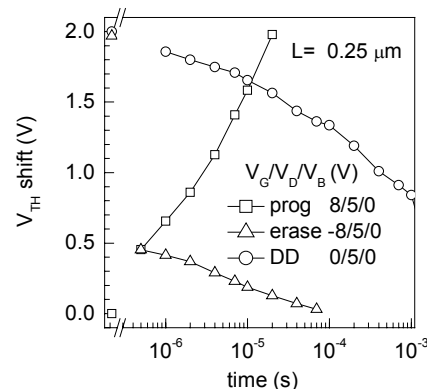


FIGURE 2. V_{TH} SHIFT OF A SONOS CELL UNDER PROGRAM, ERASE AND DRAIN DISTURB CONDITIONS.

Charge loss disturb increases with V_D as shown in Fig. 3. A programmed cell under disturb condition is in off state. Changing V_D in this condition mainly affects the fields in the drain-substrate junction and the gate-drain overlap regions. So, increased disturb at higher V_D suggests that charge transfer from or to the ONO stack takes place mainly near the drain region. This means hole injection into ONO stack from drain or electron tunneling from ONO stack to drain are the main causes for this disturb.

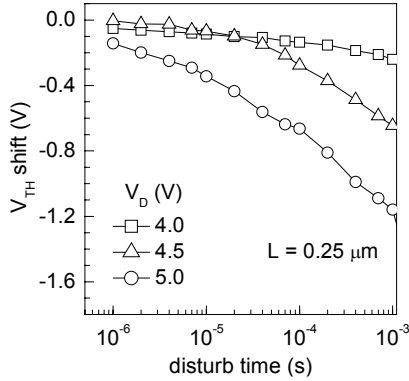


FIGURE 3. DRAIN DISTURB TRANSIENTS SHOWING THE DEPENDENCE OF V_{TH} .

It is important to note that drain coupling is absent in SONOS cells. So, the vertical field (in the channel, outside drain overlap) during disturb is mainly due to trapped charges in the ONO stack (other than V_{FB}). This could be related to the fact that SONOS cells show only charge loss disturb (from programmed state) and not charge gain disturb (from erased state). Disturb condition in a programmed cell is similar to the erase condition, with stored electrons providing the vertical field (locally).

Comparison with Erase

During erase, holes are generated from BTBT at the drain junction and are heated up in the lateral fields as they travel towards channel. These hot holes can get injected into the ONO stack under favourable fields [10]. Under disturb, the region near drain is in similar condition except that the vertical fields could be significantly different. Fig. 4 shows the Monte Carlo simulated channel hot hole density and transverse electric field along the channel (near interface) in a programmed SONOS cell under erase and disturb conditions. Similar hot hole profiles during erase and disturb suggest that BTBT generated holes could be responsible for disturb.

Charge pumping has been an important technique used to laterally profile the oxide trapped charge and interface traps in MOS devices [9,11]. It involves pulsing the channel between inversion and accumulation, and measuring the current due to recombination at the interface states to find N_{IT} . The monotonously varying V_{TH} and V_{FB} profiles along the channel (in either half of the channel) help in finding the lateral profiles of the trapped charge and the interface traps. In a SONOS cell, the ONO trapped charge can modify the V_{TH} and V_{FB} profiles along the channel, and it is not always possible to unambiguously determine the lateral profiles of trapped charge and interface traps [12]. However, charge pumping is still very useful in giving a qualitative insight into trapped charge and interface traps. Fig. 5 shows charge pumping current (I_{CP}) for two different SONOS cells. Initially, two virgin cells were programmed to the same program level (I_{CP} for one cell is shown as they both had similar I_{CP}). Then once cell was erased and other subjected to disturb (for a longer time, giving similar V_{TH} shift). The large I_{CP} increase

observed after disturb and after erase (hole injection) suggests a large increase in N_{IT} . Comparatively, there is almost no increase in the I_{CP} after program (electron injection). (The region scanned by CP is slightly decreases after program [12]) As N_{IT} generation is usually associated with the presence of holes near the interface, significant hole injection could be present during drain disturb.

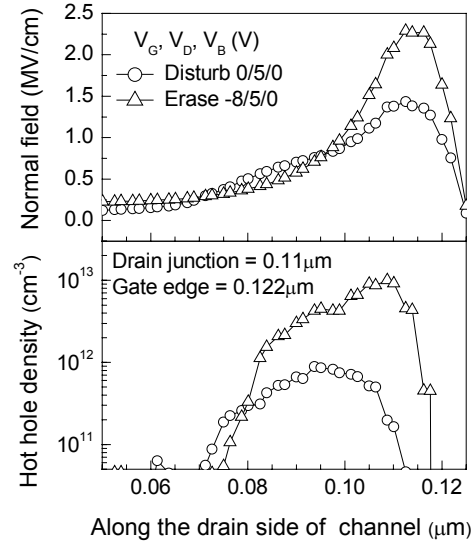


FIGURE 4. NORMAL ELECTRIC FIELD AND MONTE CARLO SIMULATED CHANNEL HOT HOLE CONCENTRATIONS UNDER ERASE AND DRAIN DISTURB CONDITIONS IN A PROGRAMMED SONOS CELL.

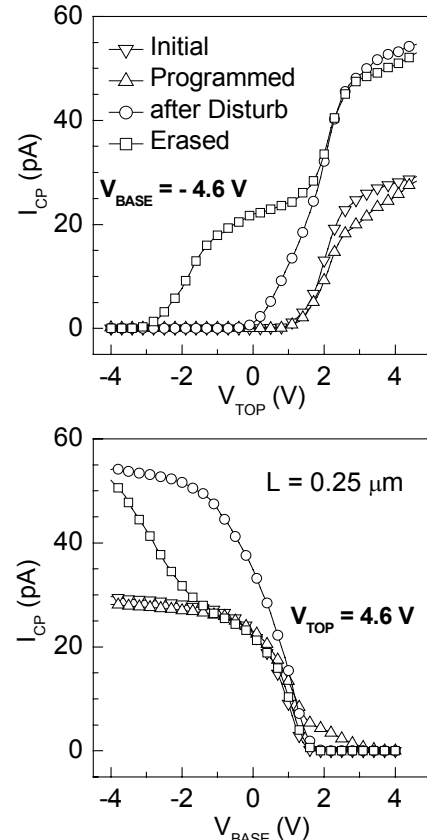


FIGURE 5. I_{CP} OF SONOS CELLS - VIRGIN, PROGRAMMED, AND AFTER DRAIN DISTURB AND ERASE.

The shift in rising edge of $I_{CP} - V_{TOP}$ curve to the left for both post-erase and post-disturb cases indicates that some region starts participating in charge pumping at much low V_{TOP} values. It can be assumed that during drain disturb, the V_{TH} and V_{FB} profiles near the source side and the center of the channel remain unaffected. Then, the observed I_{CP} is contribution of the region near drain implying that the local V_{TH} is less than that in initial or programmed cell [12]. This reduction in V_{TH} beyond the initial and programmed values indicates hole injection. Loss of injected electrons (injected during program) cannot be the dominant cause as that would never shift the rising edge of post-disturb curve beyond the initial curve. At the same time, the rising edge of $I_{CP} - V_{BASE}$ curves shifts towards the initial value, suggesting that hole injection predominantly takes place near the drain junction, where V_{FB} peaks after program [12].

BTBT taking place in the gate-drain overlap region is also known to be responsible for GIDL current [13]. BTBT generated electrons flow into the drain and the holes flow into the substrate, giving rise to the GIDL current. This BTBT in the gate-drain overlap region is exponentially dependent on the local fields. As a consequence GIDL current is very sensitive to charges near the gate-drain overlap region [14]. Fig. 6 shows GIDL characteristics measured before and after disturb along with those of pre-programmed cell. The large decrease in the GIDL current after disturb indicates a large decrease in overlap charge. In this case, it further shows that there is a large injection of holes into the ONO stack near the overlap region.

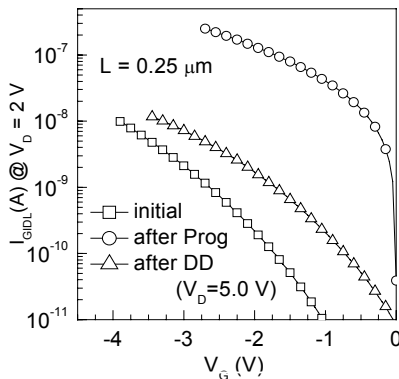


FIGURE 6. GIDL CURRENTS IN A SONOS CELL, MEASURED BEFORE AND AFTER PROGRAM, AND AFTER DRAIN DISTURB (DD) IN PROGRAM-STATE.

Mechanism of drain disturb

From the above results, drain disturb of a programmed cell can be attributed to hole injection into the ONO stack similar to that during erase. The electrons trapped in the ONO stack at the drain end provide the necessary vertical fields (both for BTBT and for injection) during disturb. To verify this, the effect of channel length (L) and channel doping on disturb is studied. BTBT is independent of L but dependent on channel doping. Memory cells with compensation implant were used for this. These show reduced BTBT as the drain-substrate junction becomes less abrupt in the channel region. Compensation implant is used to reduce natural V_{TH} (ref. Fig. 1) and increase drive current of memory cells used in embedded applications. Fig. 7 shows the effect of compensation implant and L on disturb, at different V_D . In the uncompensated cells drain disturb is very weakly dependent on L at all the V_D , which is as expected. However, drain disturb for compensated cells shows large L dependence, increasing strongly at lower L . In $0.35 \mu\text{m}$ cells, the presence of compensation changes disturb only slightly. However, in

$0.25 \mu\text{m}$ cells, addition of compensation drastically increases disturb at all V_D . This indicates the presence of another disturb component that is strongly activated at low L in compensated cells.

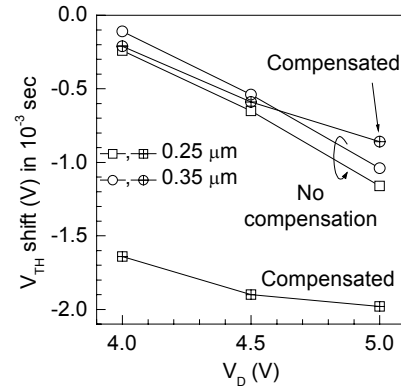


FIGURE 7. V_{TH} SHIFT DUE TO DRAIN DISTURB AT DIFFERENT L IN SONOS CELLS WITH AND WITHOUT CHANNEL COMPENSATION.

Channel leakage current could be a possible cause for this additional disturb. The presence of compensation increases the channel leakage current. It should also be noted that the localized trapping of charges in SONOS cells substantially degrades the sub-threshold slope. So, there can be substantial sub-threshold current even when the cell is programmed. These channel electrons can undergo impact ionization and generate holes, which can further get heated and injected into the ONO stack. As channel leakage current is inversely proportional to L , disturb increases at lower L .

To clarify the presence of two disturb components originating from channel leakage and BTBT, and study their relative contribution, disturb measurements were done by opening the source terminal. This would eliminate any channel current, if present. Fig 8 shows disturb transients of compensated and uncompensated cells measured with the source terminal grounded and open. Cells with compensation show a drastic reduction in disturb when the source terminal is open, indicating that channel leakage is a significant contributor to disturb in these cells. On the contrary, disturb in non-compensated cells changes very little when source is open, indicating a negligible contribution from channel leakage.

The opposing dependence of BTBT and channel leakage current on V_B can also be used to verify their contribution to disturb. Fig 9a shows disturb transients at different V_B . Making V_B more negative increases BTBT but decreases channel leakage current (due to body-effect). Disturb increases with increasing $|V_B|$ in uncompensated cells showing BTBT as the dominant cause for disturb in these cells. Disturb decreases with $|V_B|$ in compensated cells showing channel leakage as the dominant component leading to disturb. However, the latter is true only at short L as channel leakage reduces at larger L , even in compensated cells. Fig. 9b shows V_{TH} shift due to disturb as a function of V_B for different L . Only short L , compensated cell shows improvement in drain disturb as $|V_B|$ is increased.

These results clearly show that drain disturb in a programmed SONOS cell can be caused by injection of holes that originate from two different sources. The main source is the BTBT taking place in the drain at the gate-drain overlap region. The other source is the channel leakage current, which can undergo impact ionization. The latter can become dominant in cells with low V_{TH} or significant sub-threshold slope degradation, at low L .

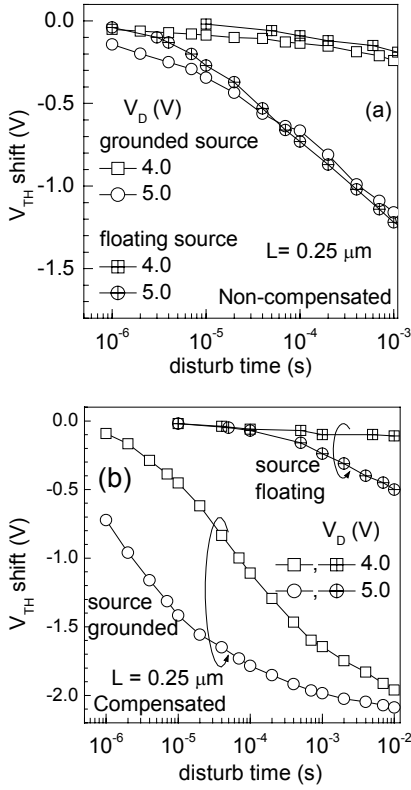


FIGURE 8. DRAIN DISTURB TRANSIENTS WITH SOURCE TERMINAL GROUNDED AND OPEN, AT DIFFERENT V_D IN SONOS CELLS WITHOUT (a) AND WITH (b) COMPENSATION IMPLANT.

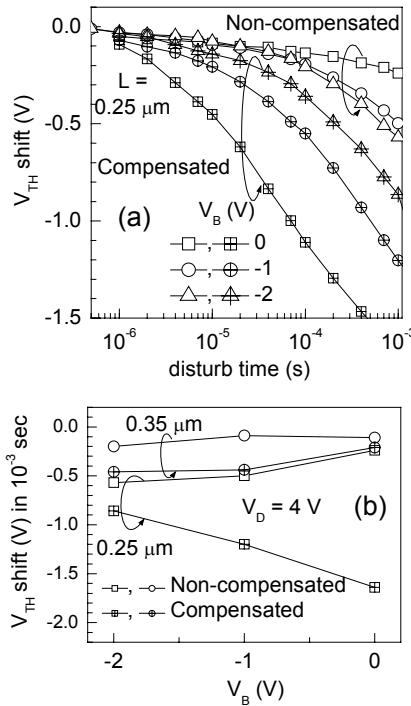


FIGURE 9. (a) DRAIN DISTURB TRANSIENTS IN SONOS CELLS AS A FUNCTION OF V_B , AND (b) V_{TH} SHIFT DUE TO DRAIN DISTURB AS A FUNCTION OF V_B AT DIFFERENT L IN CELLS WITH AND WITHOUT COMPENSATION.

Finally, the effect of halo doping on disturb is studied. Halo implants are known to increase the program efficiency in flash cells due to the higher fields near the drain junction. They also increase BTBT and hot-hole generation for a given V_D [6]. Fig. 10 shows drain disturb transients under different V_D on non-compensated cells with and without halo doping. Presence of halo increases the disturb at all V_D . This further proves that BTBT is the dominant cause of disturb in non-compensated cells.

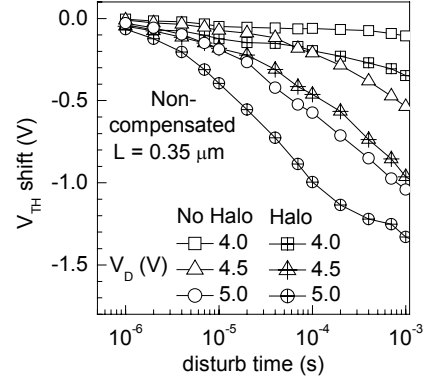


FIGURE 10. THE EFFECT OF HALO DOPING ON DRAIN DISTURB TRANSIENTS AT DIFFERENT V_D , IN NON-COMPENSATED SONOS CELLS.

CONCLUSION

Program drain disturb in SONOS cells is investigated. Hot hole injection from substrate into the nitride is found to be the main cause for charge loss drain disturb seen in programmed cells. BTBT at the gate-drain overlap region and channel leakage are identified as the two key mechanisms responsible for generation of these holes. BTBT dominates for non-compensated cells with and without halo doping for all L and compensated cells at large L . Channel leakage dominates for compensated cells at smaller L and can cause severe bottleneck for cell scaling. The drain disturb condition studied here can occur even during erase (done by HHI), if bit-by-bit erase is performed.

ACKNOWLEDGMENT

The authors would like to thank Jeff Bude (Agere Systems, USA) for providing the Monte Carlo simulator.

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