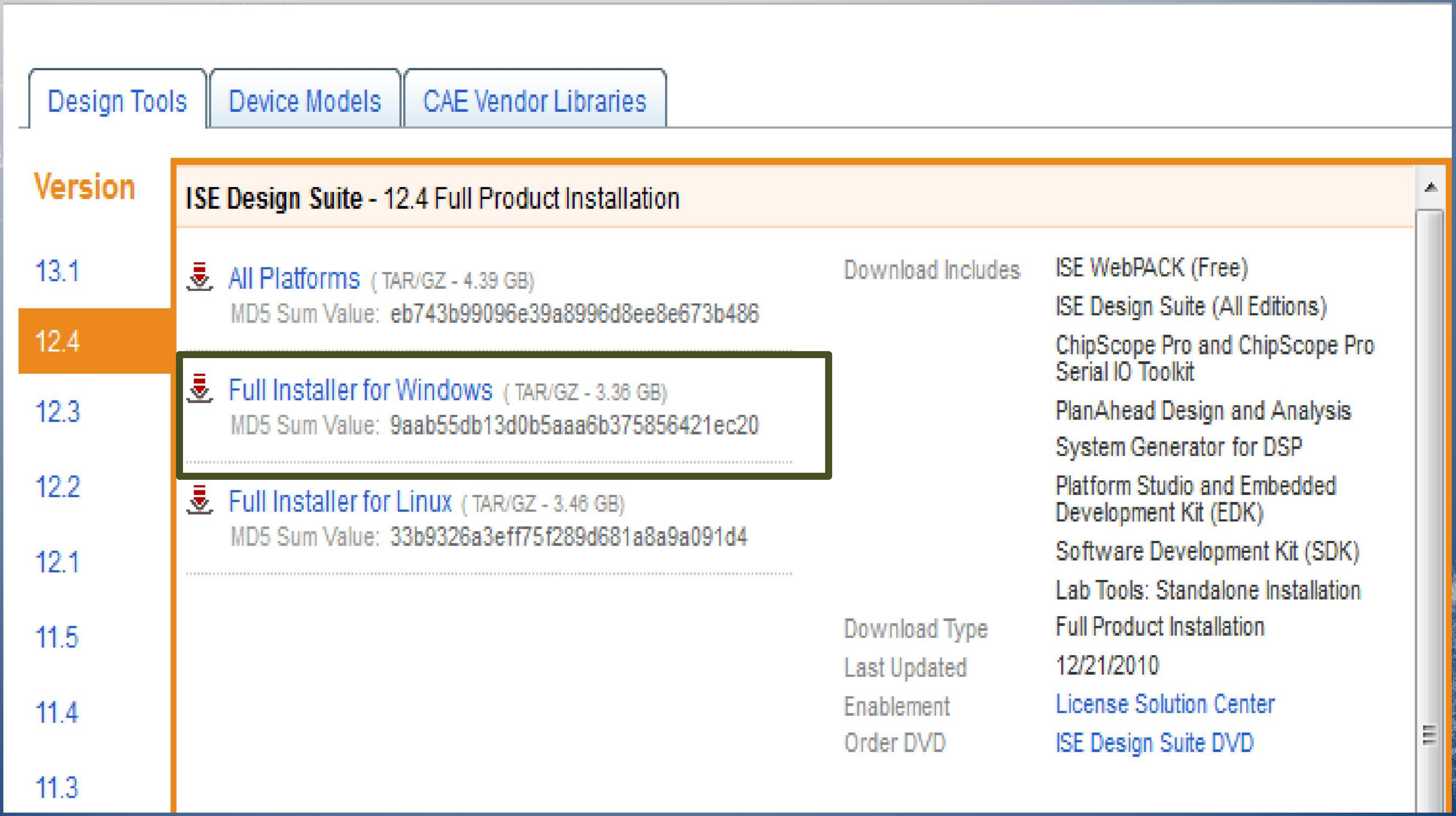
This Tutorial of Xilinx ISE is only for CML Members

Part I: ISE12.4 Installation

Download ISE12.4 on Xilinx Webpage:

http://www.xilinx.com/support/download/index.htm



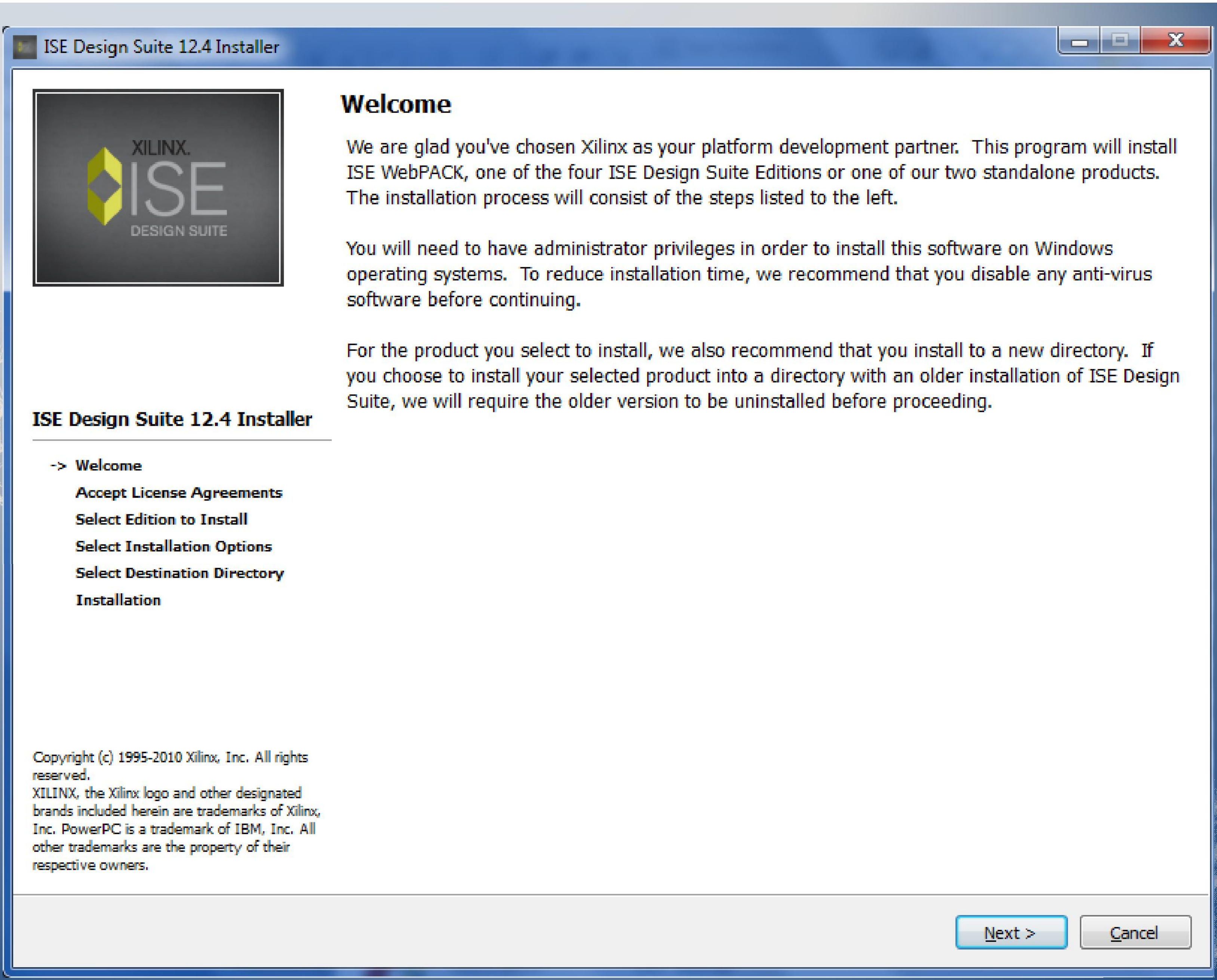
ISE Design Suite - 12.4 Full Product Installation

All Platforms (TAR/GZ - 4.39 GB)
MD5 Sum Value: eb743b99096e39a8996d8ee8e673b486

Full Installer for Windows (TAR/GZ - 3.38 GB)
MD5 Sum Value: 9aab55db13d0b5aaa6b375856421ec20

Full Installer for Linux (TAR/GZ - 3.46 GB)
MD5 Sum Value: 33b9326a3eff75f289d681a8a9a091d4

Download Includes	ISE WebPACK (Free) ISE Design Suite (All Editions) ChipScope Pro and ChipScope Pro Serial IO Toolkit PlanAhead Design and Analysis System Generator for DSP Platform Studio and Embedded Development Kit (EDK) Software Development Kit (SDK) Lab Tools: Standalone Installation
Download Type	Full Product Installation
Last Updated	12/21/2010
Enablement	License Solution Center
Order DVD	ISE Design Suite DVD



Welcome

We are glad you've chosen Xilinx as your platform development partner. This program will install ISE WebPACK, one of the four ISE Design Suite Editions or one of our two standalone products. The installation process will consist of the steps listed to the left.

You will need to have administrator privileges in order to install this software on Windows operating systems. To reduce installation time, we recommend that you disable any anti-virus software before continuing.

For the product you select to install, we also recommend that you install to a new directory. If you choose to install your selected product into a directory with an older installation of ISE Design Suite, we will require the older version to be uninstalled before proceeding.

ISE Design Suite 12.4 Installer

- -> **Welcome**
- **Accept License Agreements**
- **Select Edition to Install**
- **Select Installation Options**
- **Select Destination Directory**
- **Installation**

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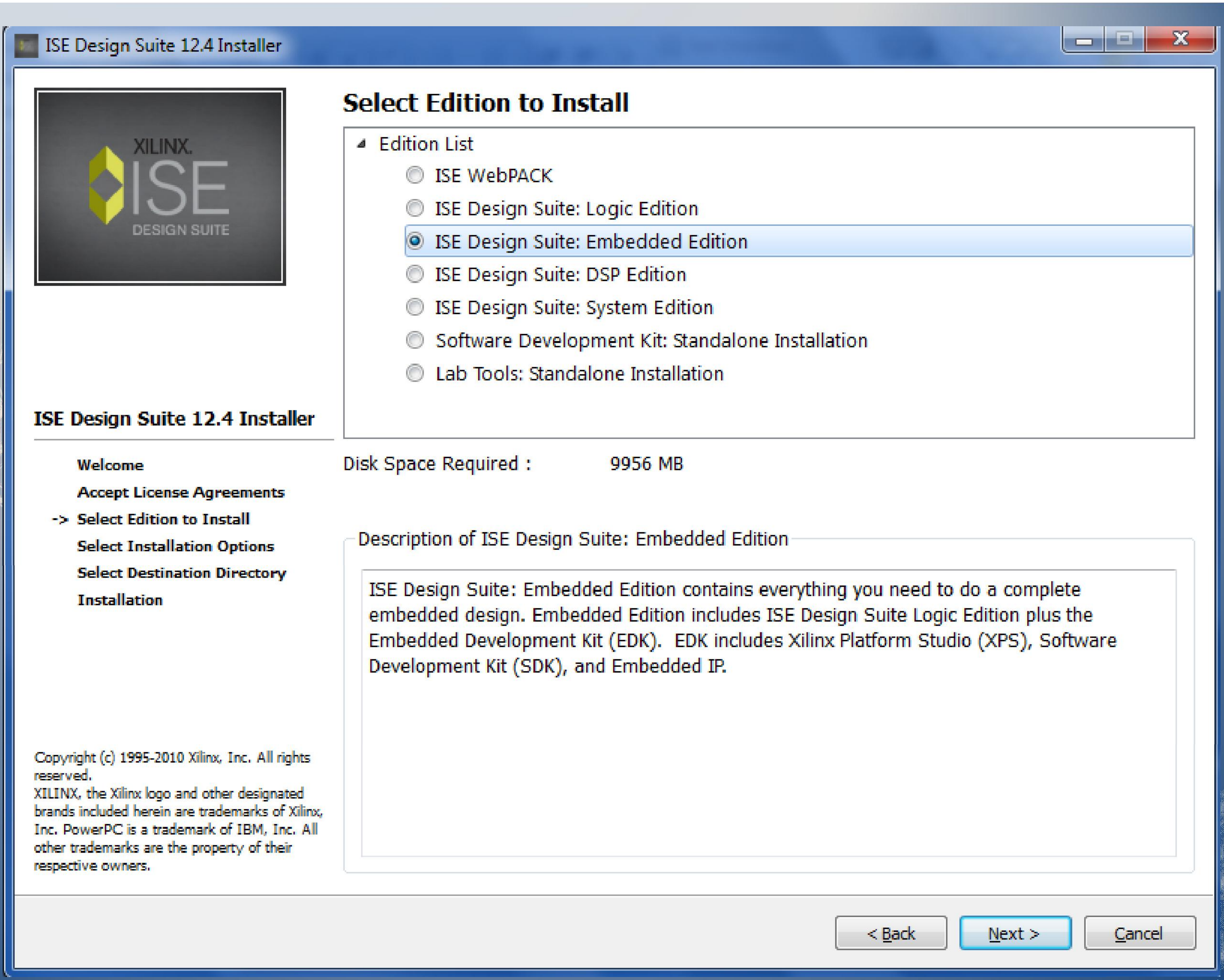
Install Mainpage-------Click Next



Select Edition to Install

Edition List

- ○ ISE WebPACK
- ○ ISE Design Suite: Logic Edition
- ● ISE Design Suite: Embedded Edition
- ○ ISE Design Suite: DSP Edition
- ○ ISE Design Suite: System Edition
- ○ Software Development Kit: Standalone Installation
- ○ Lab Tools: Standalone Installation

Disk Space Required : 9956 MB

Description of ISE Design Suite: Embedded Edition

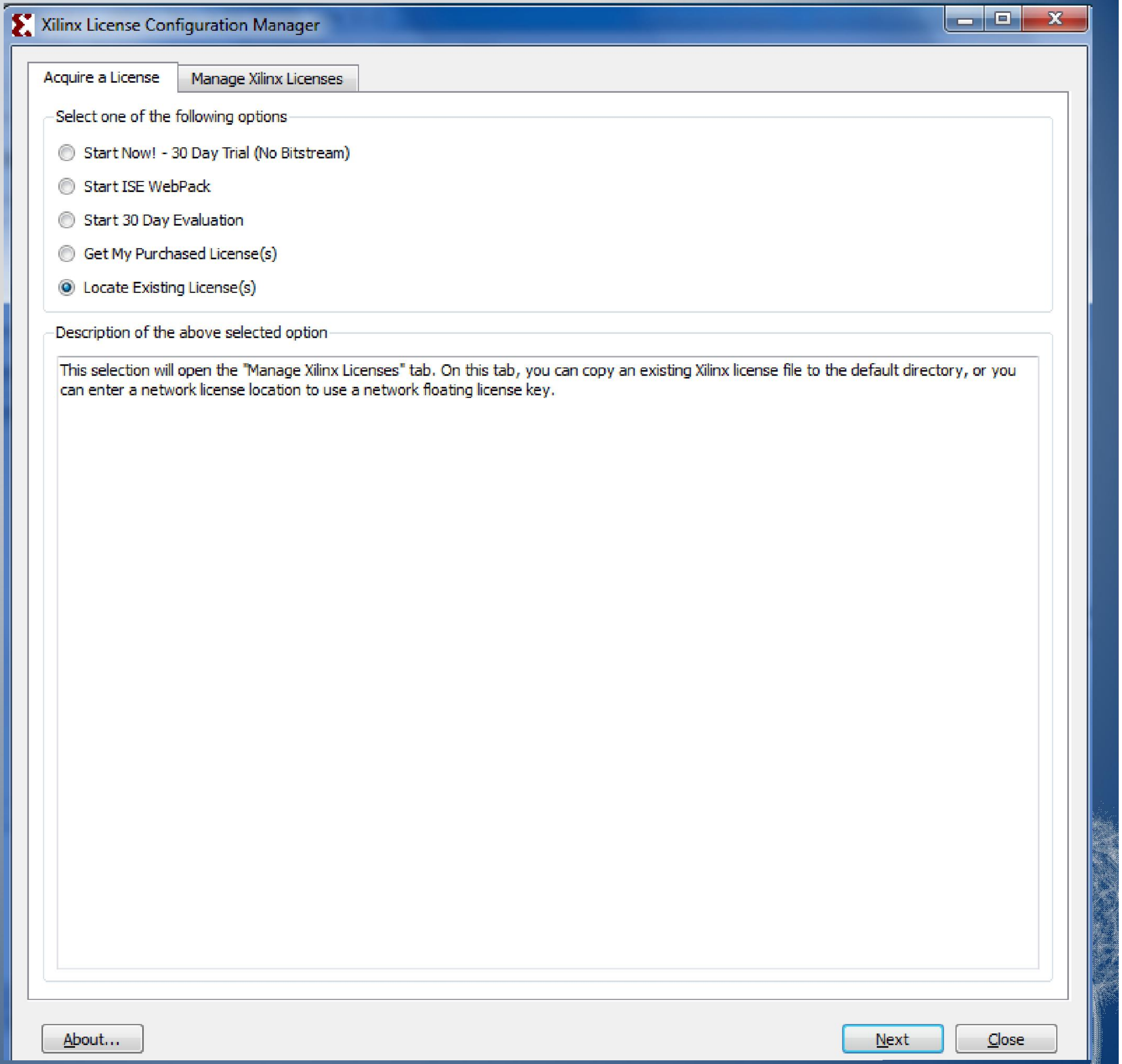
ISE Design Suite: Embedded Edition contains everything you need to do a complete embedded design. Embedded Edition includes ISE Design Suite Logic Edition plus the Embedded Development Kit (EDK). EDK includes Xilinx Platform Studio (XPS), Software Development Kit (SDK), and Embedded IP.

ISE Design Suite 12.4 Installer

- Welcome
- Accept License Agreements
- -> Select Edition to Install
- Select Installation Options
- Select Destination Directory
- Installation

This step has a trick: Please choose Embedded Edition, then Click Next and Begin Install

After Installation, you should make the License Configuration, choose Locate Existing Licenses, then Click Next



Xilinx License Configuration Manager

Select one of the following options

○ Start Now! - 30 Day Trial (No Bitstream)

○ Start ISE WebPack

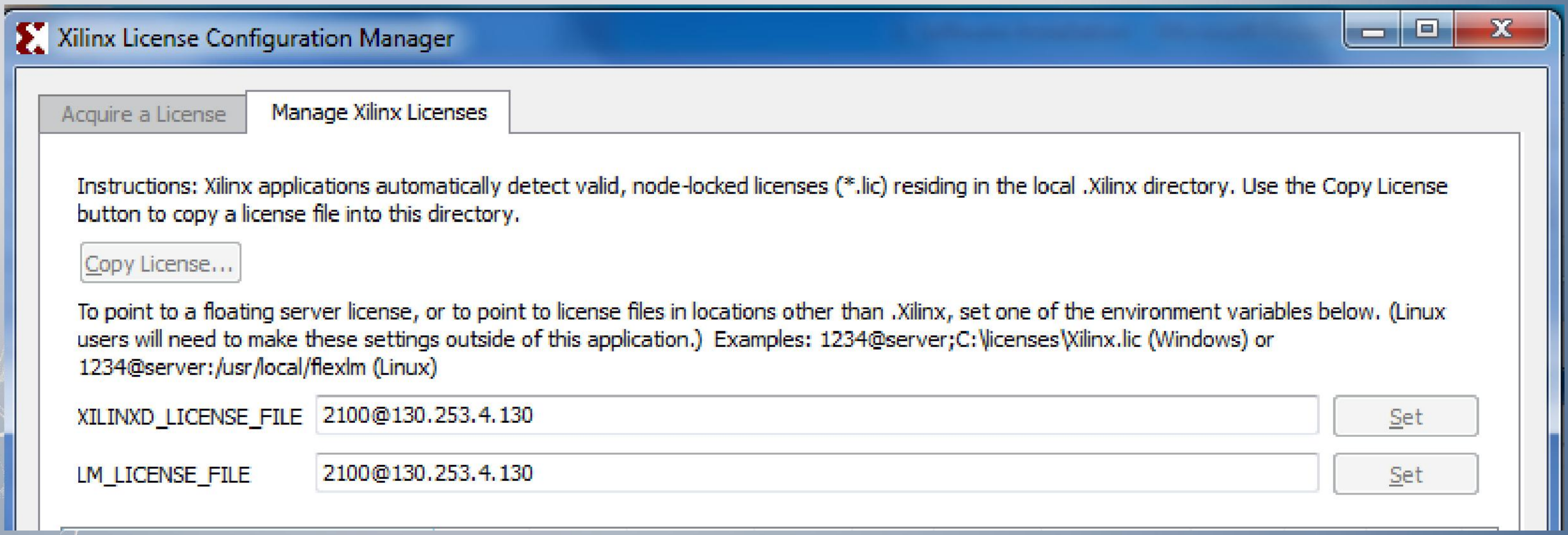
○ Start 30 Day Evaluation

○ Get My Purchased License(s)

● Locate Existing License(s)

Description of the above selected option

This selection will open the "Manage Xilinx Licenses" tab. On this tab, you can copy an existing Xilinx license file to the default directory, or you can enter a network license location to use a network floating license key.



Instructions: Xilinx applications automatically detect valid, node-locked licenses (*.lic) residing in the local .Xilinx directory. Use the Copy License button to copy a license file into this directory.

To point to a floating server license, or to point to license files in locations other than .Xilinx, set one of the environment variables below. (Linux users will need to make these settings outside of this application.) Examples: 1234@server;C:\licenses\Xilinx.lic (Windows) or 1234@server:/usr/local/flexlm (Linux)

XILINXD_LICENSE_FILE 2100@130.253.4.130

LM_LICENSE_FILE 2100@130.253.4.130

One the blank row, input 2100@130.253.4.130
This is license Dr. Voyles bought for CML.

After License Configuration, you can try ISE 12.4 according to the next part tutorial

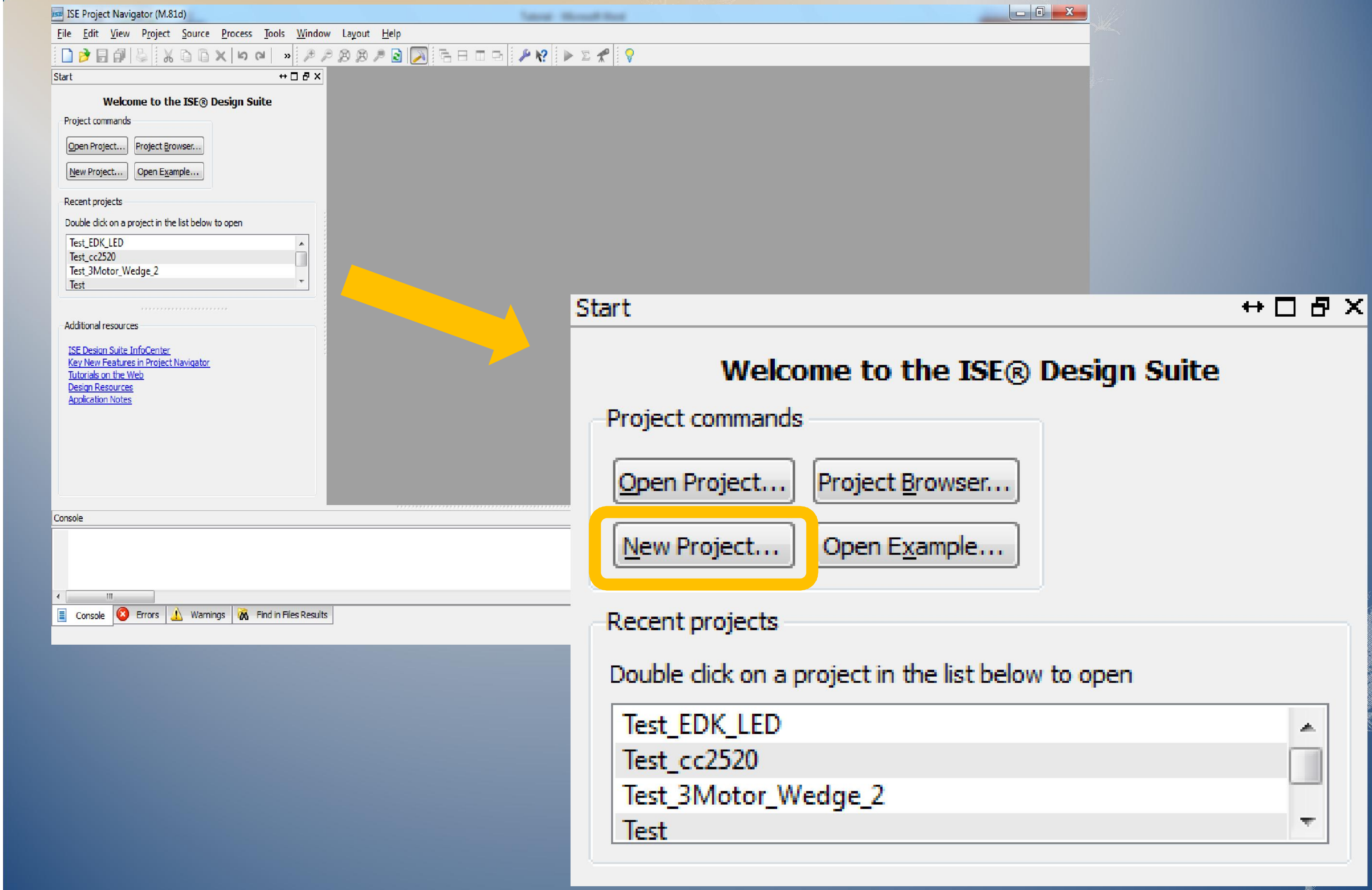
Part II:
Create a Project in ISE 12.4

This tutorial will show you how to recreate a project in EDK with some files in the folder.

Part 1 is about creating a new project in ISE.

Part 2 is about adding IPs cores to the project in the XPS, including the IPs xilinx provided and IPs user created.

Part 3 is about creating software projects in the SDK, writing codes and downloading them into the FPGA.



Start

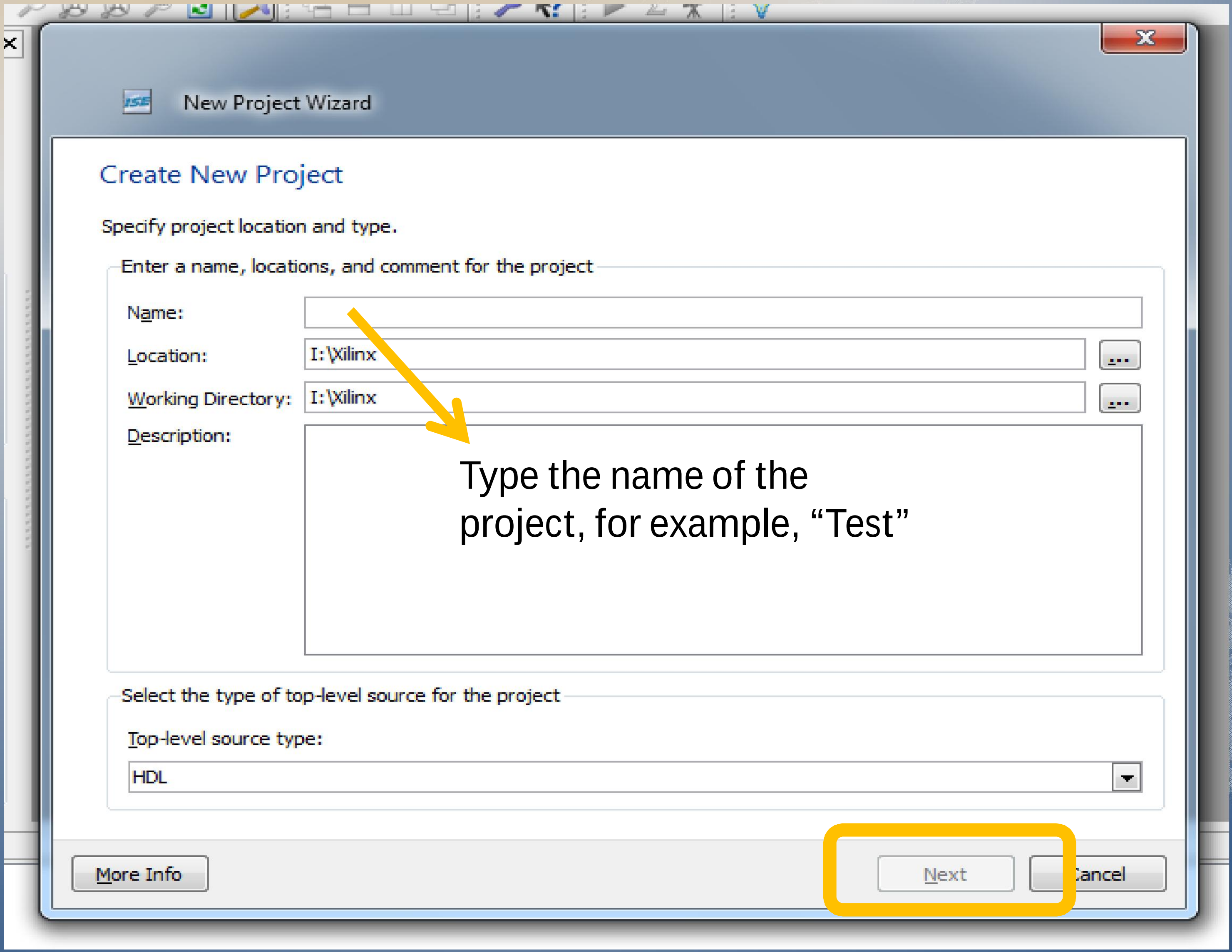
Welcome to the ISE® Design Suite

Project commands

Recent projects

Double click on a project in the list below to open

Test_EDK_LED
Test_cc2520
Test_3Motor_Wedge_2
Test



New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name:

Location: I:\Xilinx

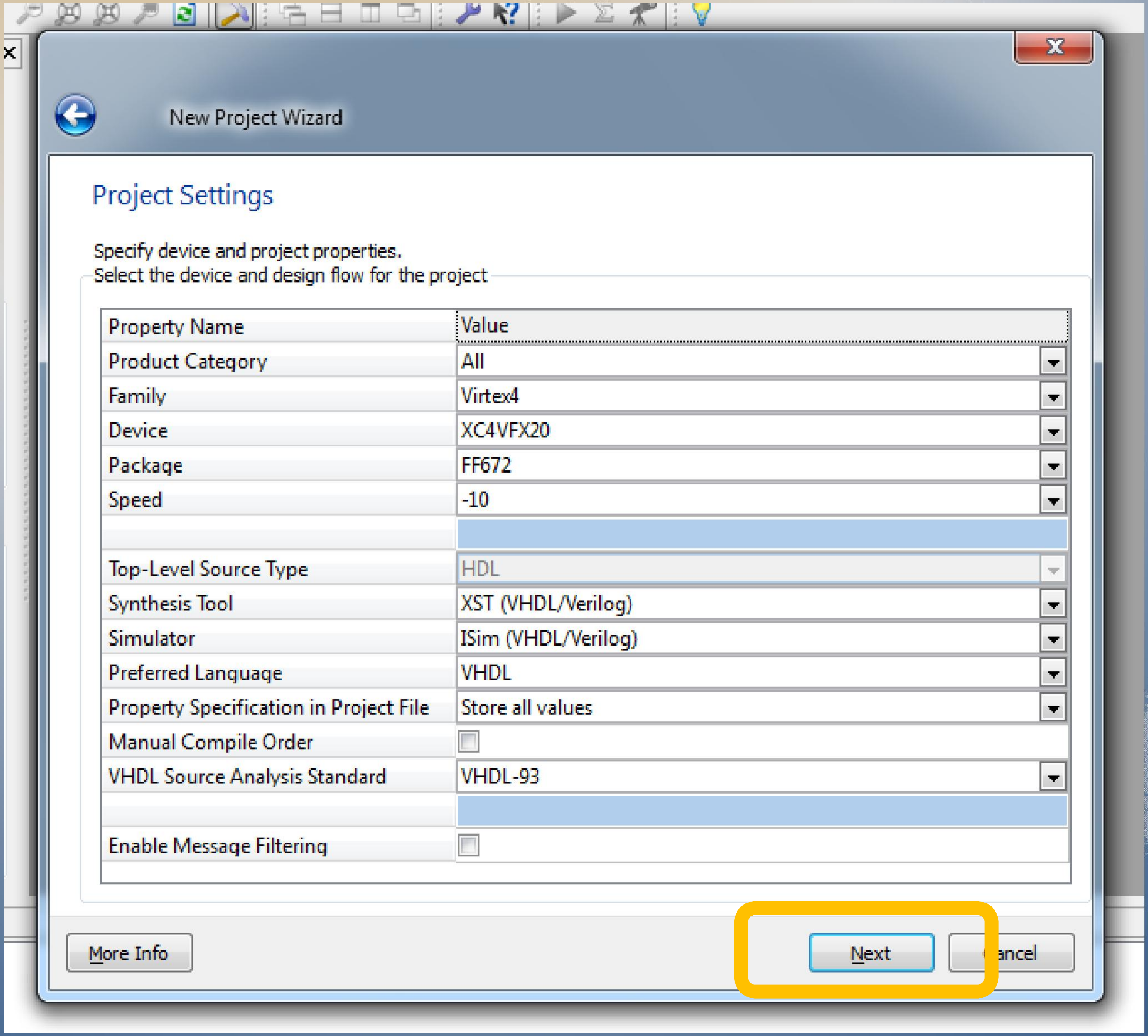
Working Directory: I:\Xilinx

Description:

Select the type of top-level source for the project

Top-level source type: HDL

Type the name of the project, for example, “Test”

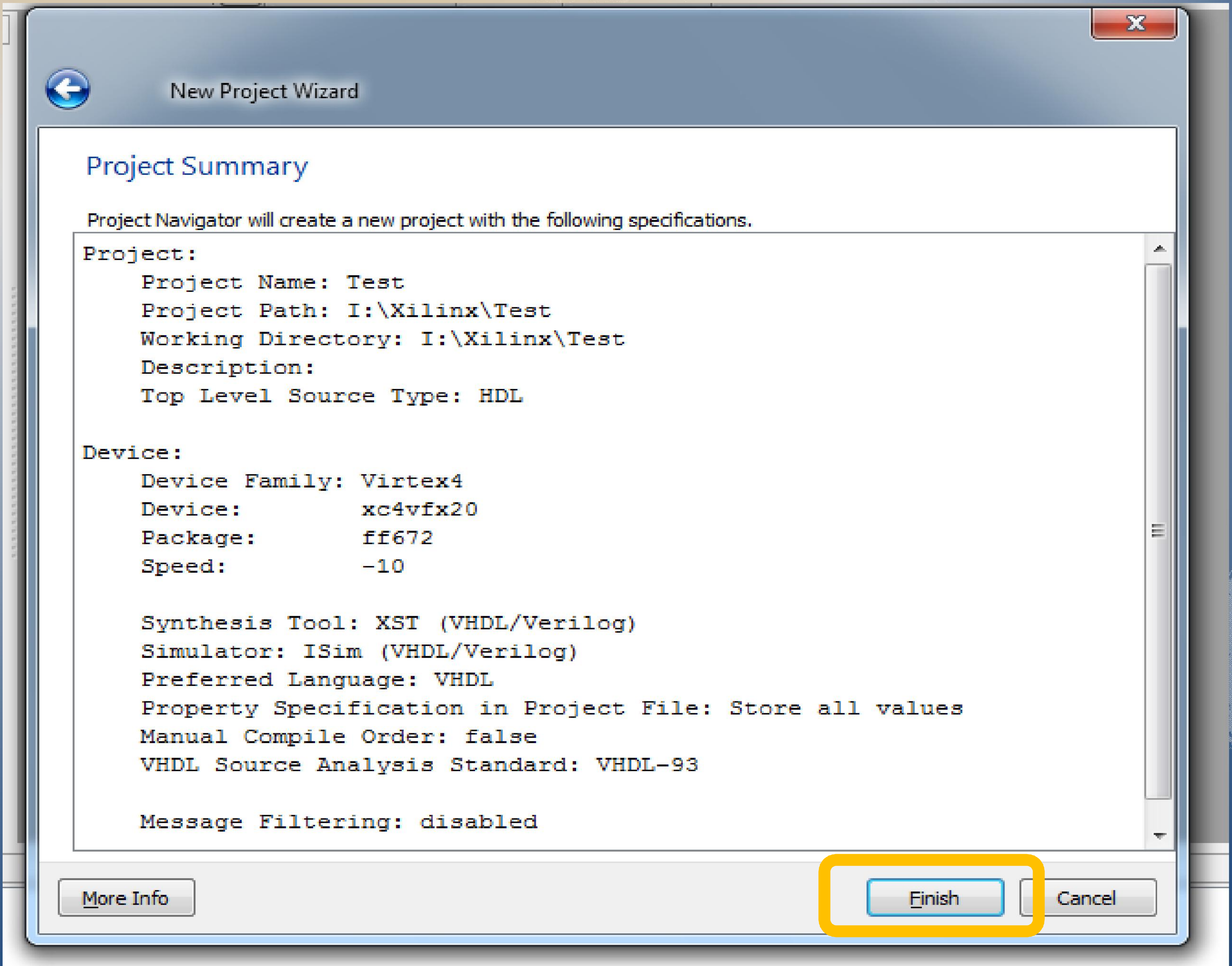


Project Settings

Specify device and project properties.

Select the device and design flow for the project

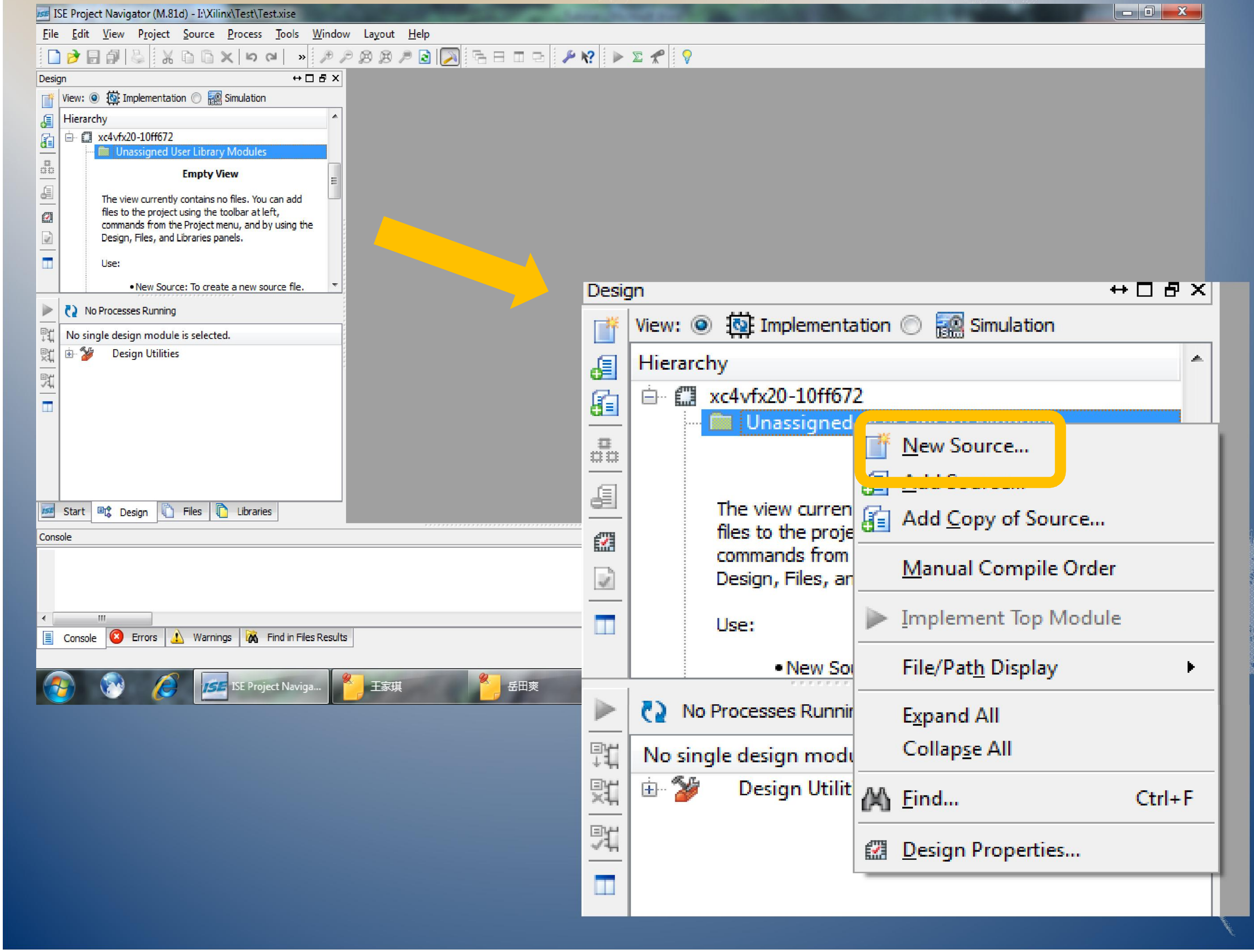
Property Name	Value
Product Category	All
Family	Virtex4
Device	XC4VFX20
Package	FF672
Speed	-10
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	□
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	□



Project Summary

Project Navigator will create a new project with the following specifications.

```
Project:
    Project Name: Test
    Project Path: I:\Xilinx\Test
    Working Directory: I:\Xilinx\Test
    Description:
    Top Level Source Type: HDL

Device:
    Device Family: Virtex4
    Device:        xc4vfx20
    Package:       ff672
    Speed:         -10

    Synthesis Tool: XST (VHDL/Verilog)
    Simulator: ISim (VHDL/Verilog)
    Preferred Language: VHDL
    Property Specification in Project File: Store all values
    Manual Compile Order: false
    VHDL Source Analysis Standard: VHDL-93

    Message Filtering: disabled
```



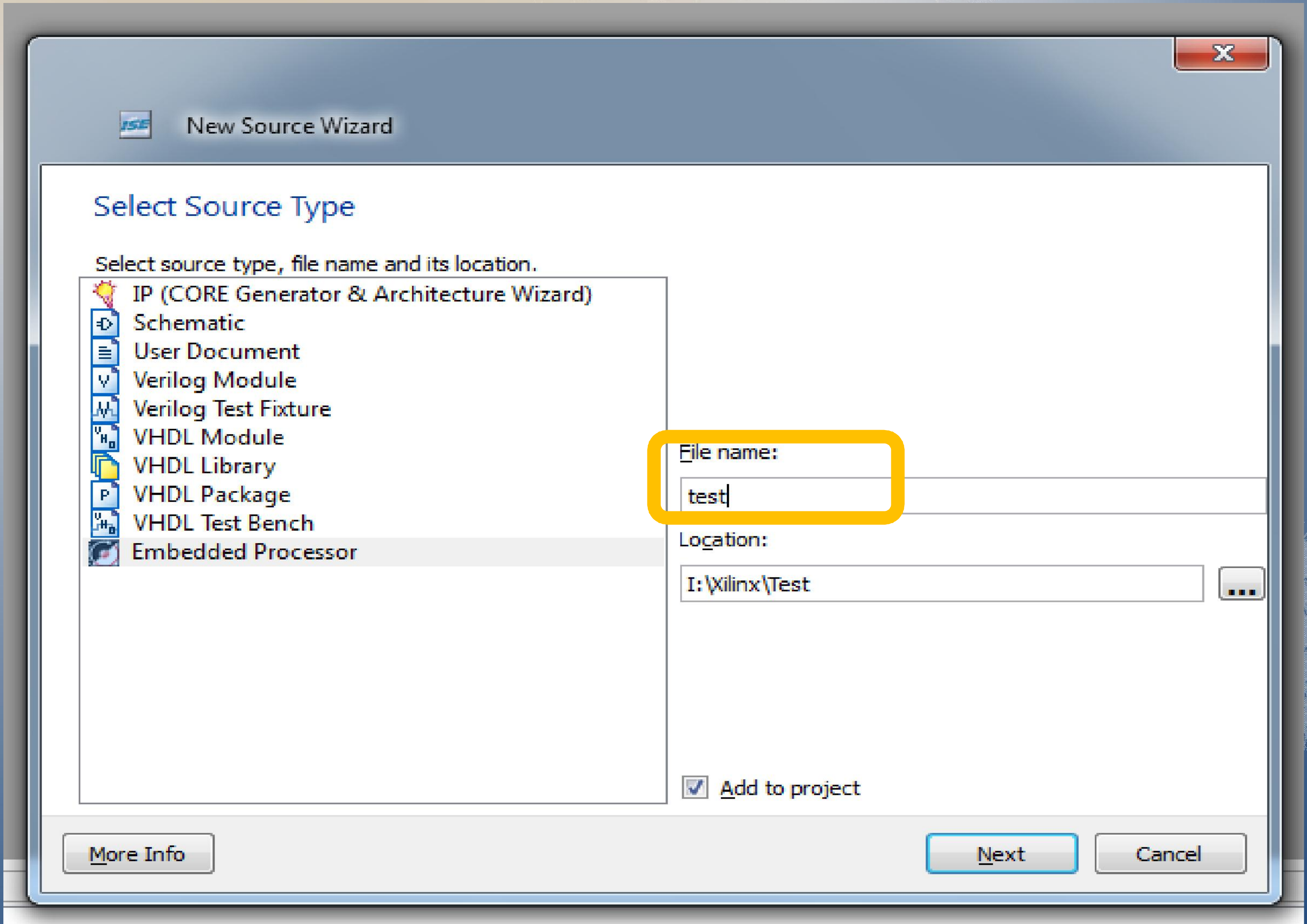
Empty View

The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.

Use:

- New Source: To create a new source file.

No single design module is selected.



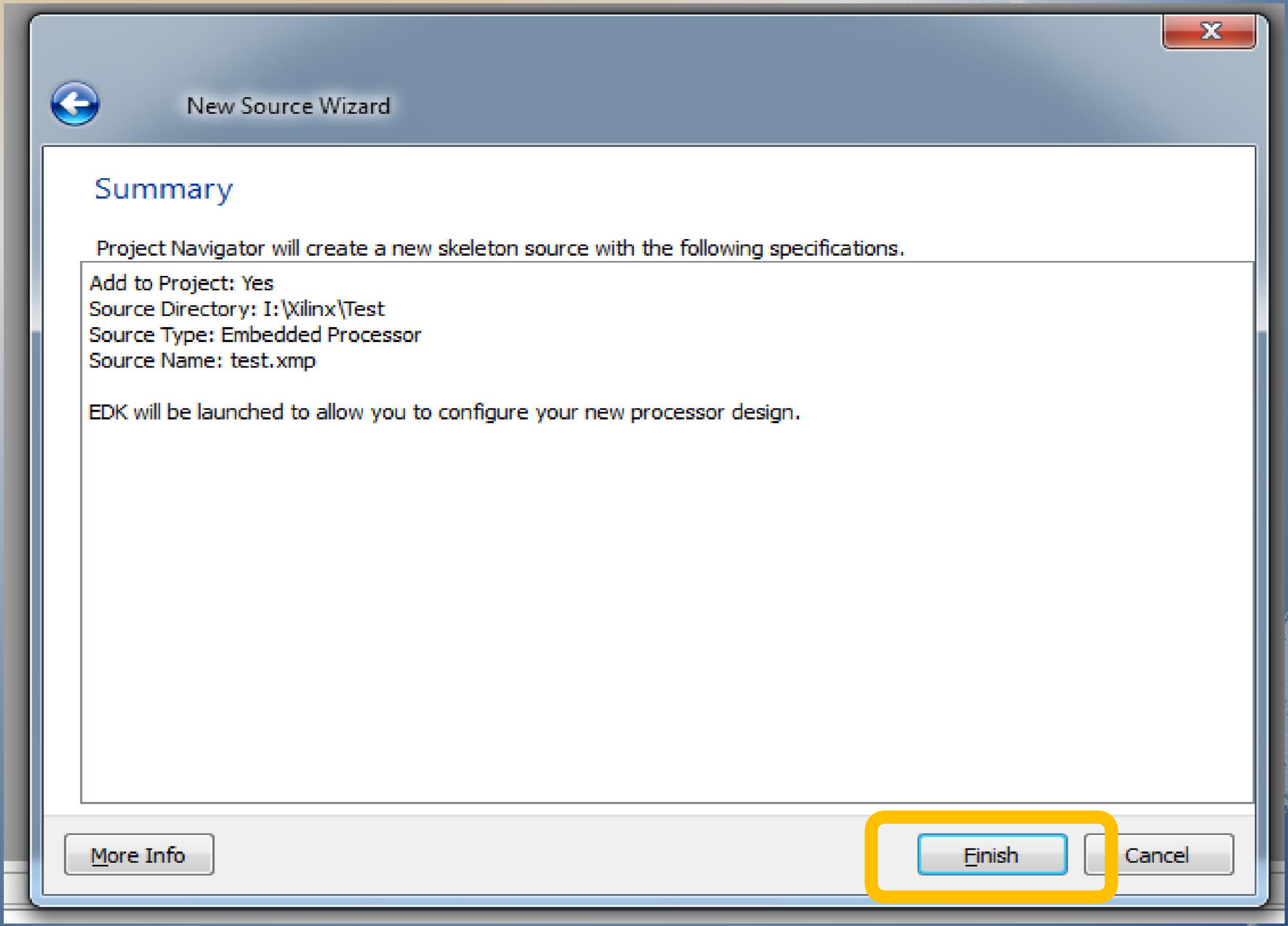
Select Source Type

Select source type, file name and its location.

File name: test

Location: I:\Xilinx\Test

☑ Add to project

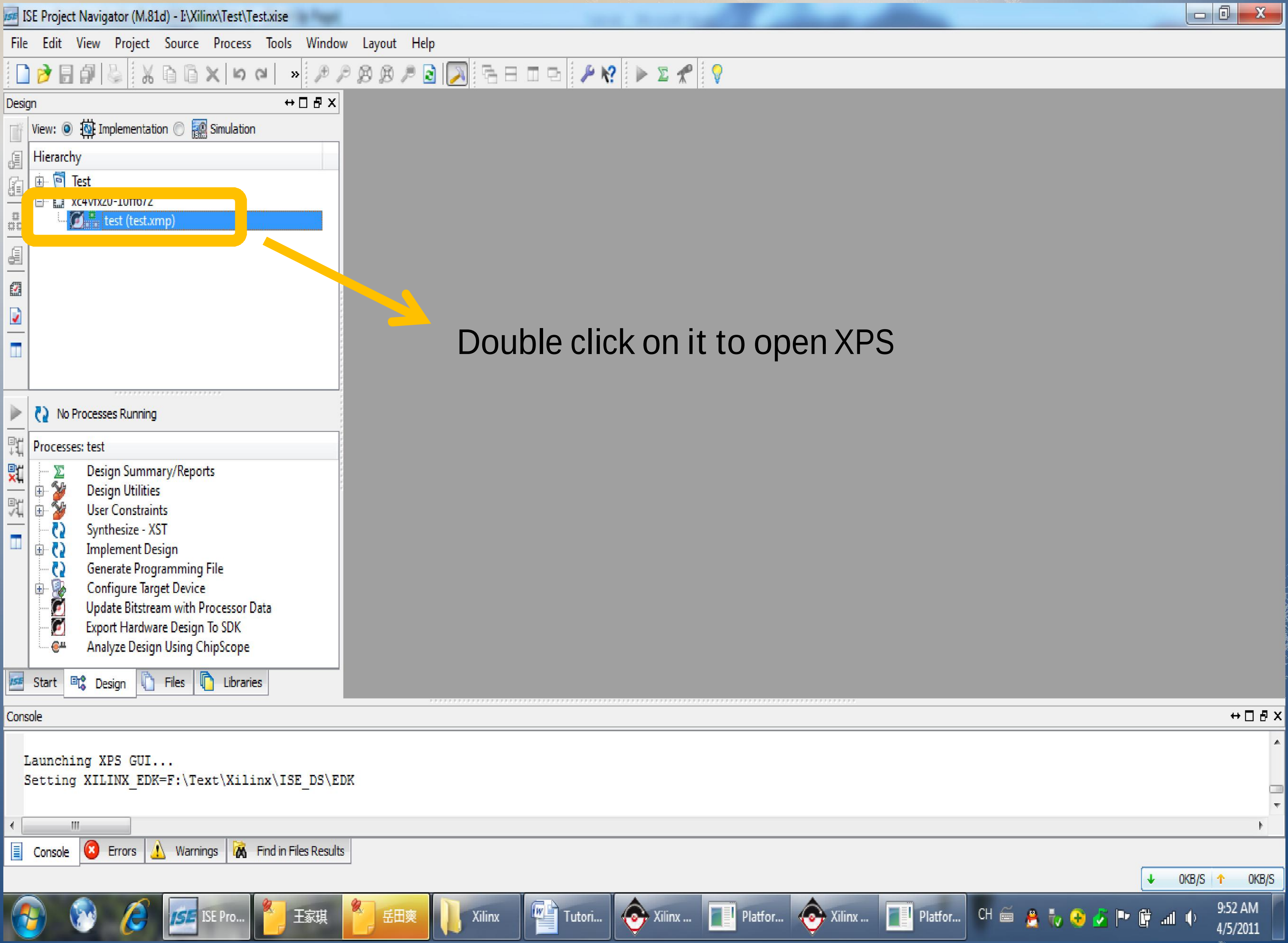


Summary

Project Navigator will create a new skeleton source with the following specifications.

Add to Project: Yes
Source Directory: I:\Xilinx\Test
Source Type: Embedded Processor
Source Name: test.xmp

EDK will be launched to allow you to configure your new processor design.

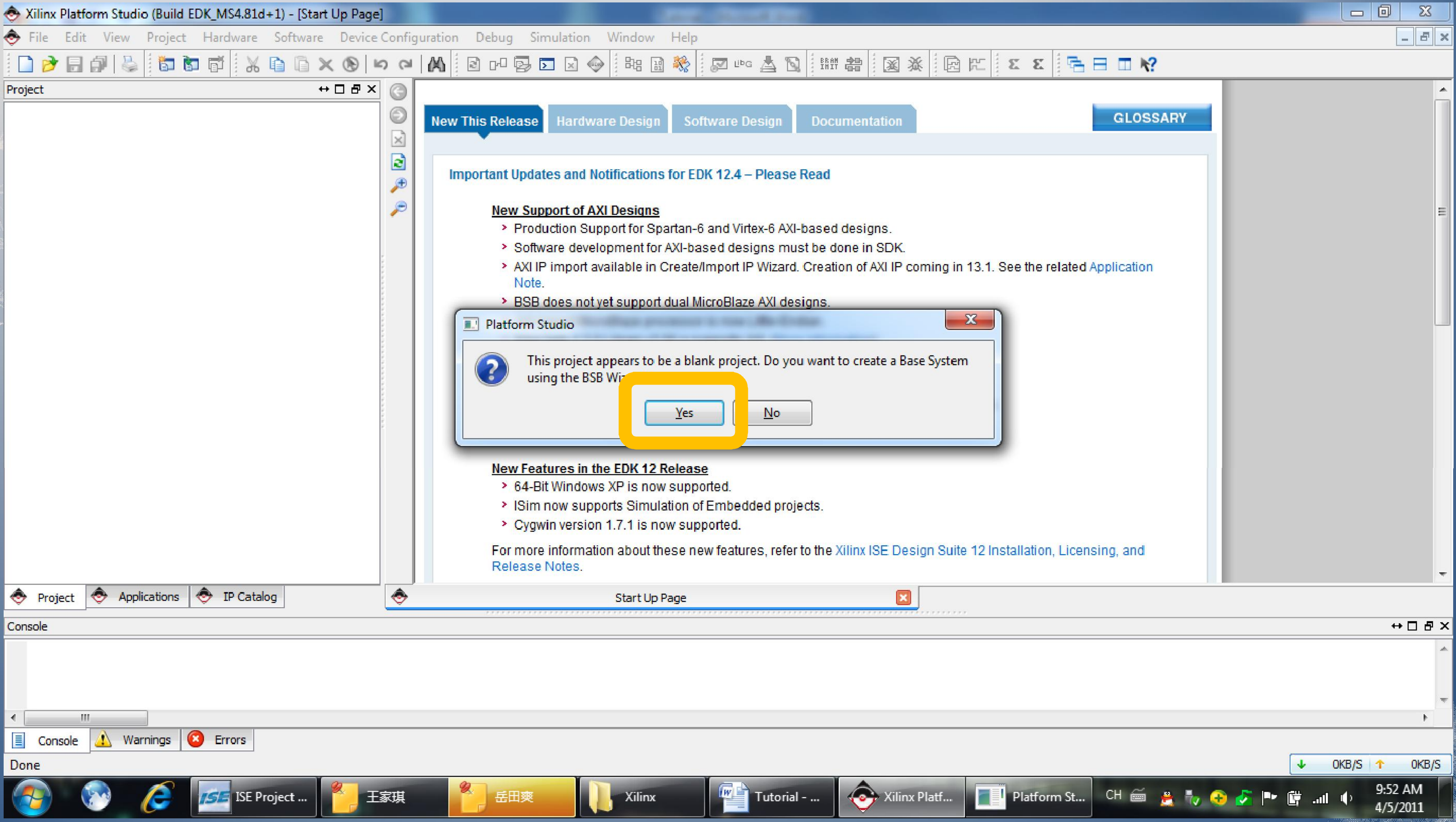


Double click on it to open XPS

```
Launching XPS GUI...
Setting XILINX_EDK=F:\Text\Xilinx\ISE_DS\EDK
```

Part III: Add IP cores in XPS

This part will show you how to add IP cores in XPS. Several IPs will be added, including a LEDs_4Bit IP, a general purpose IO IP, and three MOTOR_WEDGE IP .



Important Updates and Notifications for EDK 12.4 – Please Read

New Support of AXI Designs

- Production Support for Spartan-6 and Virtex-6 AXI-based designs.
- Software development for AXI-based designs must be done in SDK.
- AXI IP import available in Create/Import IP Wizard. Creation of AXI IP coming in 13.1. See the related Application Note.
- BSB does not yet support dual MicroBlaze AXI designs.

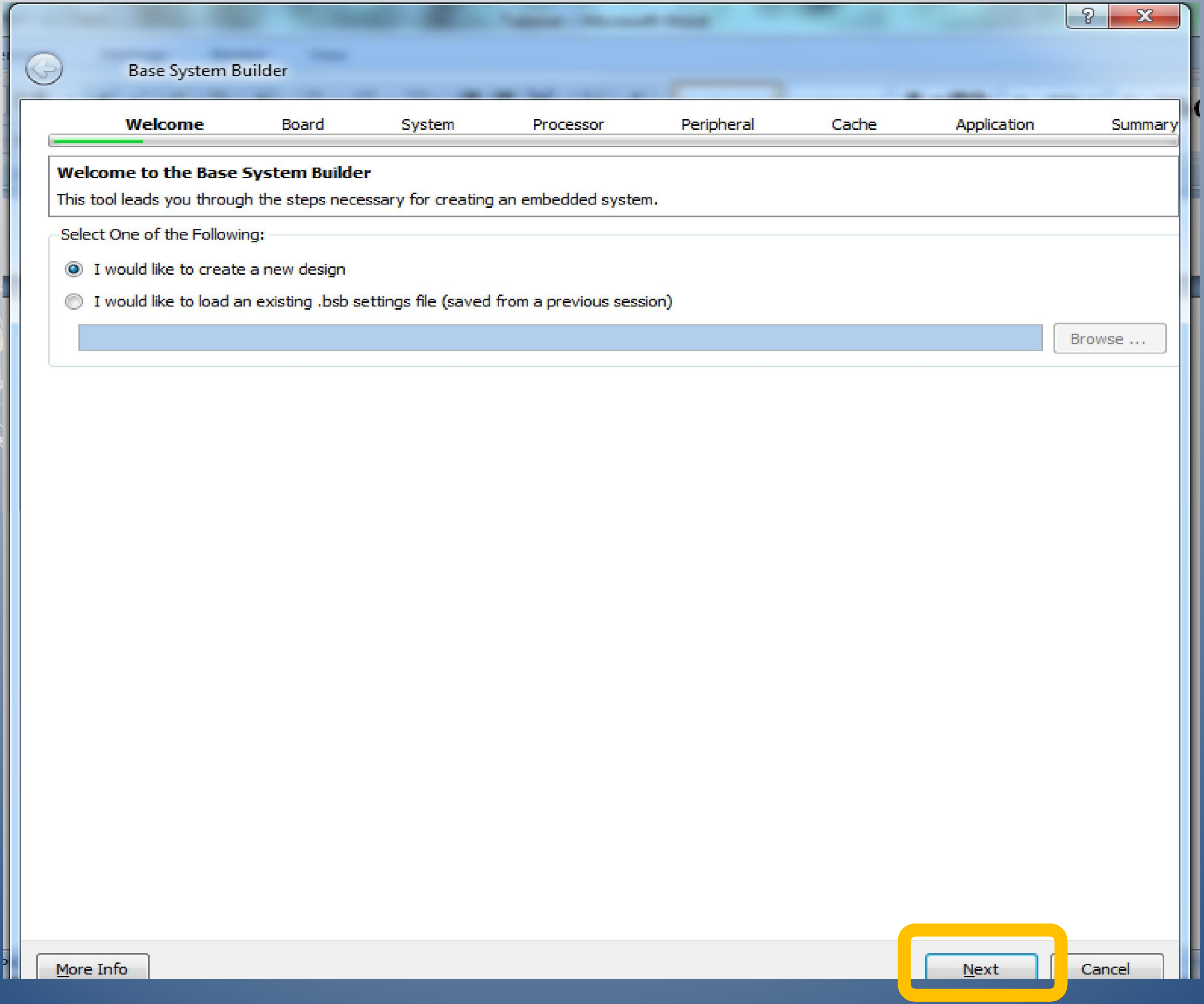
Platform Studio

This project appears to be a blank project. Do you want to create a Base System using the BSB Wi

New Features in the EDK 12 Release

- 64-Bit Windows XP is now supported.
- ISim now supports Simulation of Embedded projects.
- Cygwin version 1.7.1 is now supported.

For more information about these new features, refer to the Xilinx ISE Design Suite 12 Installation, Licensing, and Release Notes.



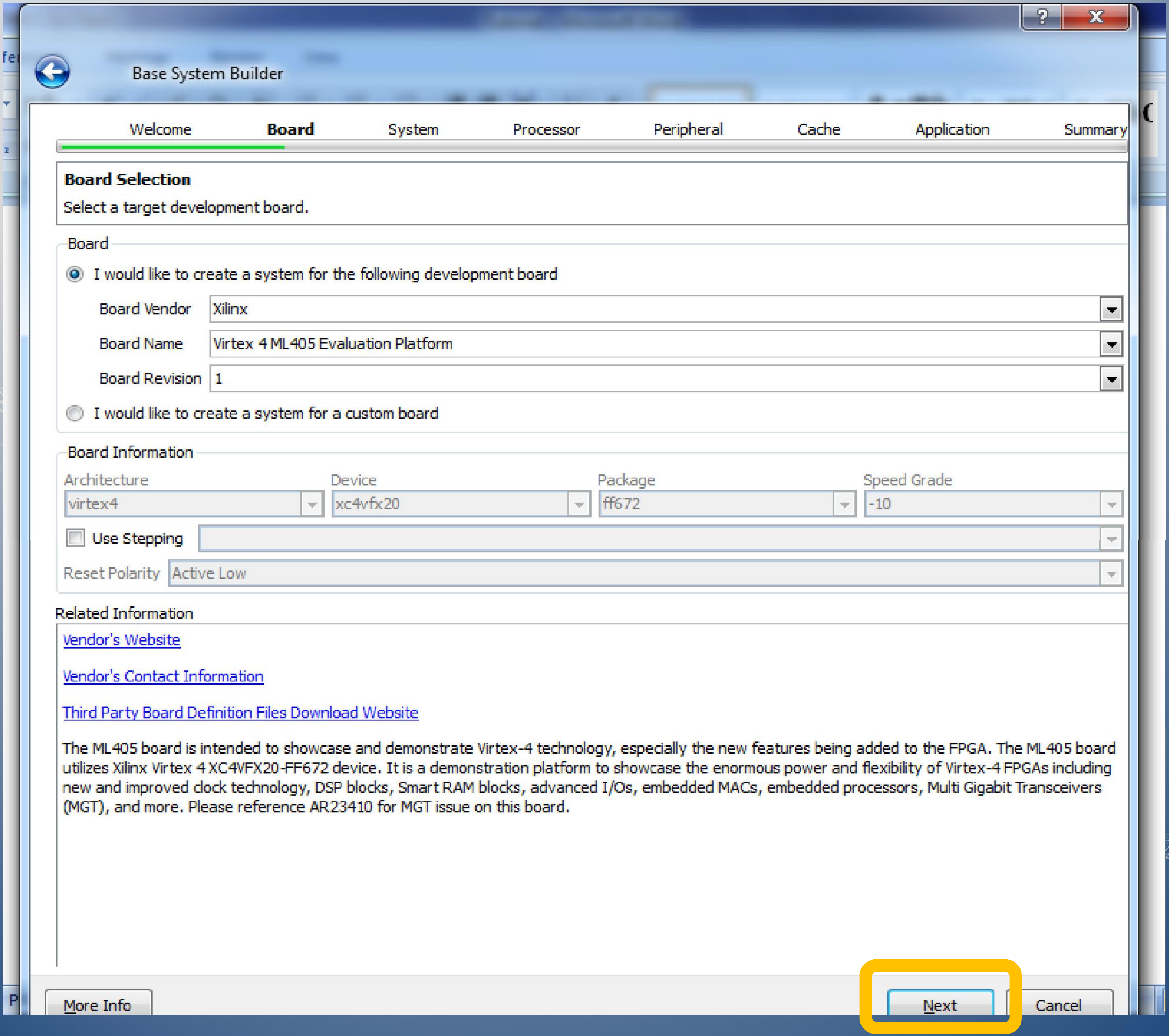
Welcome to the Base System Builder

This tool leads you through the steps necessary for creating an embedded system.

Select One of the Following:

● I would like to create a new design

○ I would like to load an existing .bsb settings file (saved from a previous session)



Board Selection

Select a target development board.

Board

● I would like to create a system for the following development board

Board Vendor: Xilinx

Board Name: Virtex 4 ML405 Evaluation Platform

Board Revision: 1

○ I would like to create a system for a custom board

Board Information

Architecture	Device	Package	Speed Grade
virtex4	xc4vfx20	ff672	-10

□ Use Stepping

Reset Polarity: Active Low

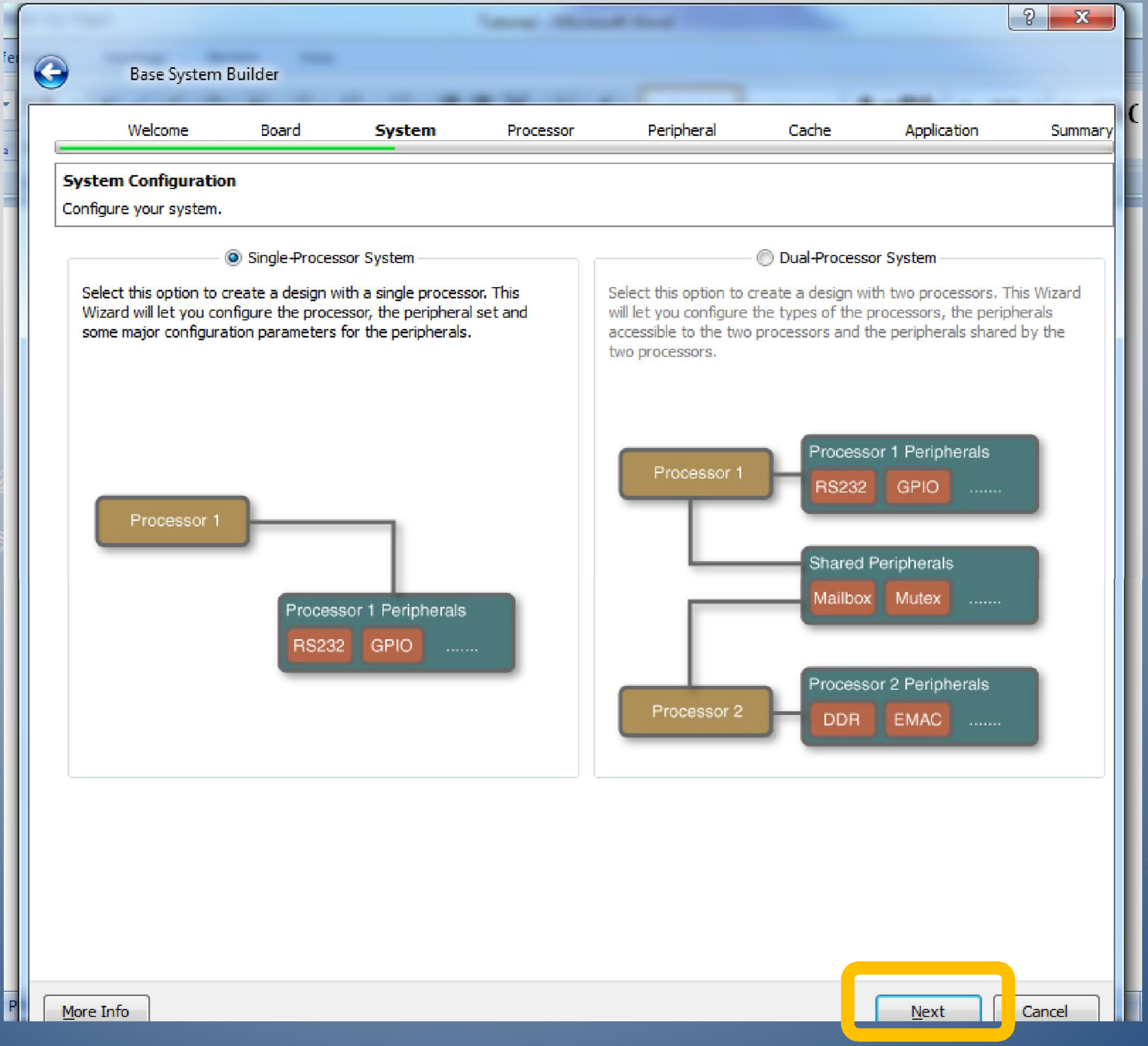
Related Information

Vendor's Website

Vendor's Contact Information

Third Party Board Definition Files Download Website

The ML405 board is intended to showcase and demonstrate Virtex-4 technology, especially the new features being added to the FPGA. The ML405 board utilizes Xilinx Virtex 4 XC4VFX20-FF672 device. It is a demonstration platform to showcase the enormous power and flexibility of Virtex-4 FPGAs including new and improved clock technology, DSP blocks, Smart RAM blocks, advanced I/Os, embedded MACs, embedded processors, Multi Gigabit Transceivers (MGT), and more. Please reference AR23410 for MGT issue on this board.



System Configuration

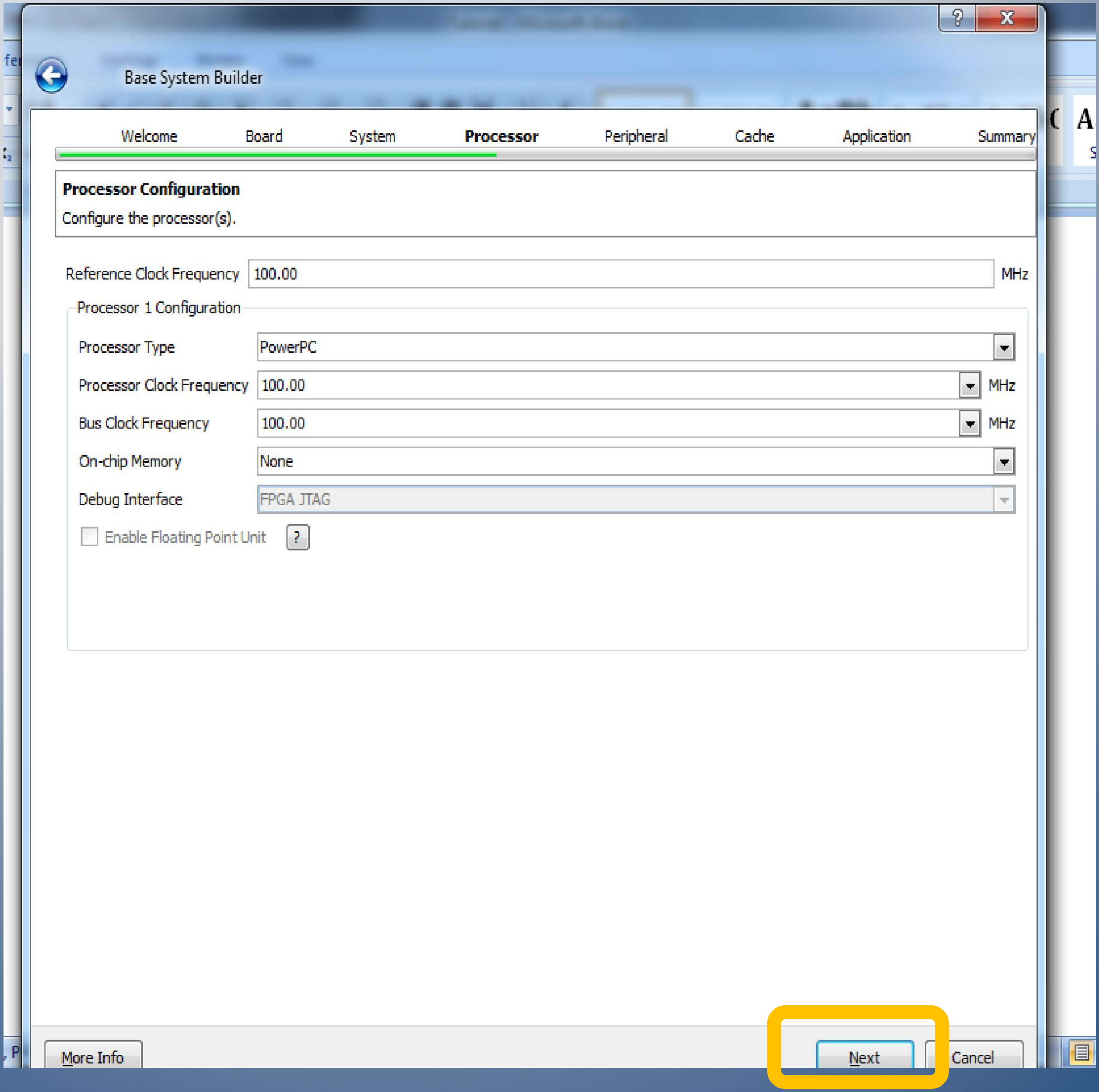
Configure your system.

● Single-Processor System

Select this option to create a design with a single processor. This Wizard will let you configure the processor, the peripheral set and some major configuration parameters for the peripherals.

○ Dual-Processor System

Select this option to create a design with two processors. This Wizard will let you configure the types of the processors, the peripherals accessible to the two processors and the peripherals shared by the two processors.



Base System Builder

Processor Configuration

Configure the processor(s).

Reference Clock Frequency 100.00 MHz

Processor 1 Configuration

Processor Type PowerPC

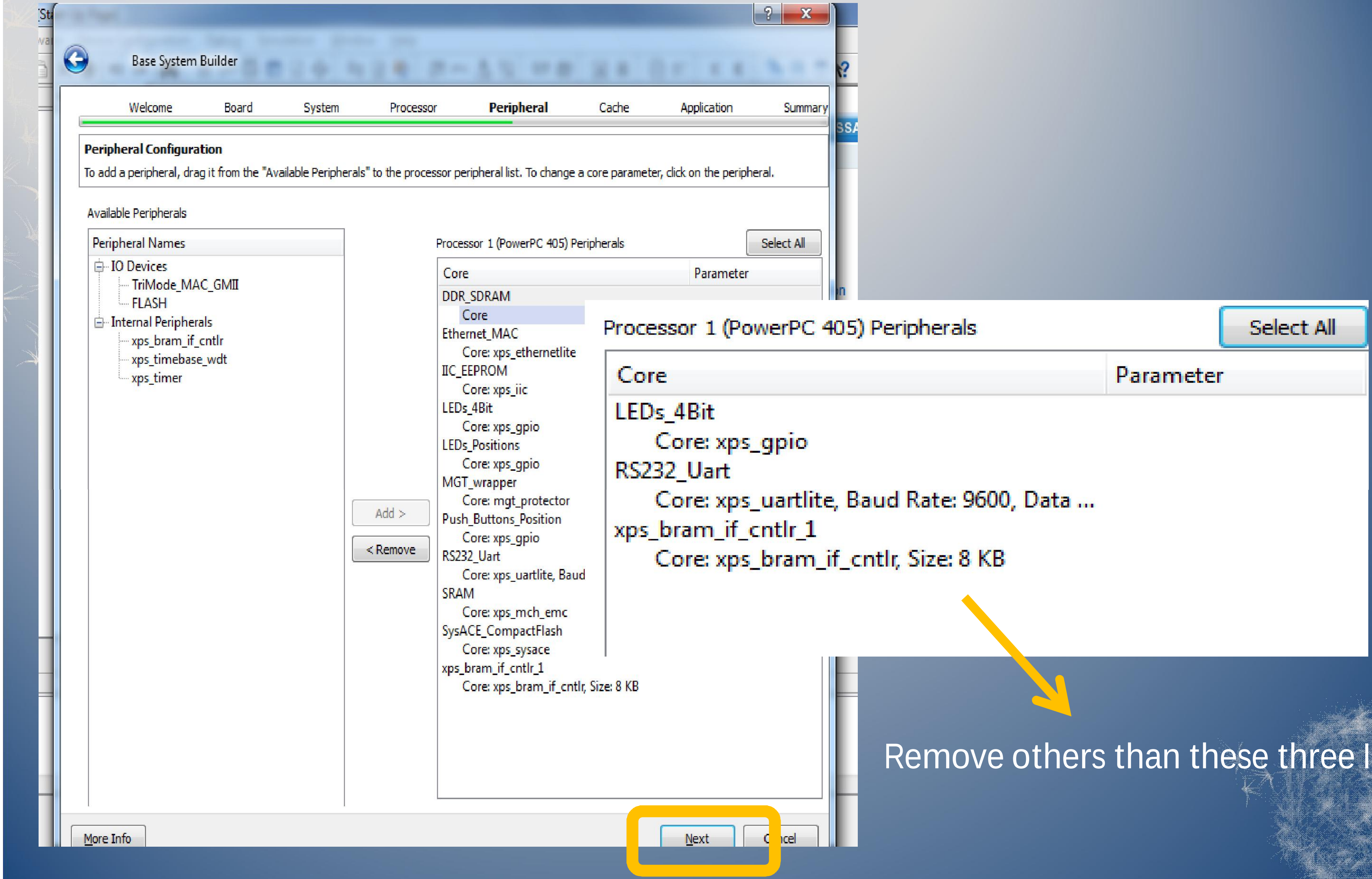
Processor Clock Frequency 100.00 MHz

Bus Clock Frequency 100.00 MHz

On-chip Memory None

Debug Interface FPGA JTAG

□ Enable Floating Point Unit



Peripheral Configuration

To add a peripheral, drag it from the "Available Peripherals" to the processor peripheral list. To change a core parameter, click on the peripheral.

Available Peripherals

Peripheral Names
- IO Devices
  - TriMode_MAC_GMII
  - FLASH
- Internal Peripherals
  - xps_bram_if_cntlr
  - xps_timebase_wdt
  - xps_timer

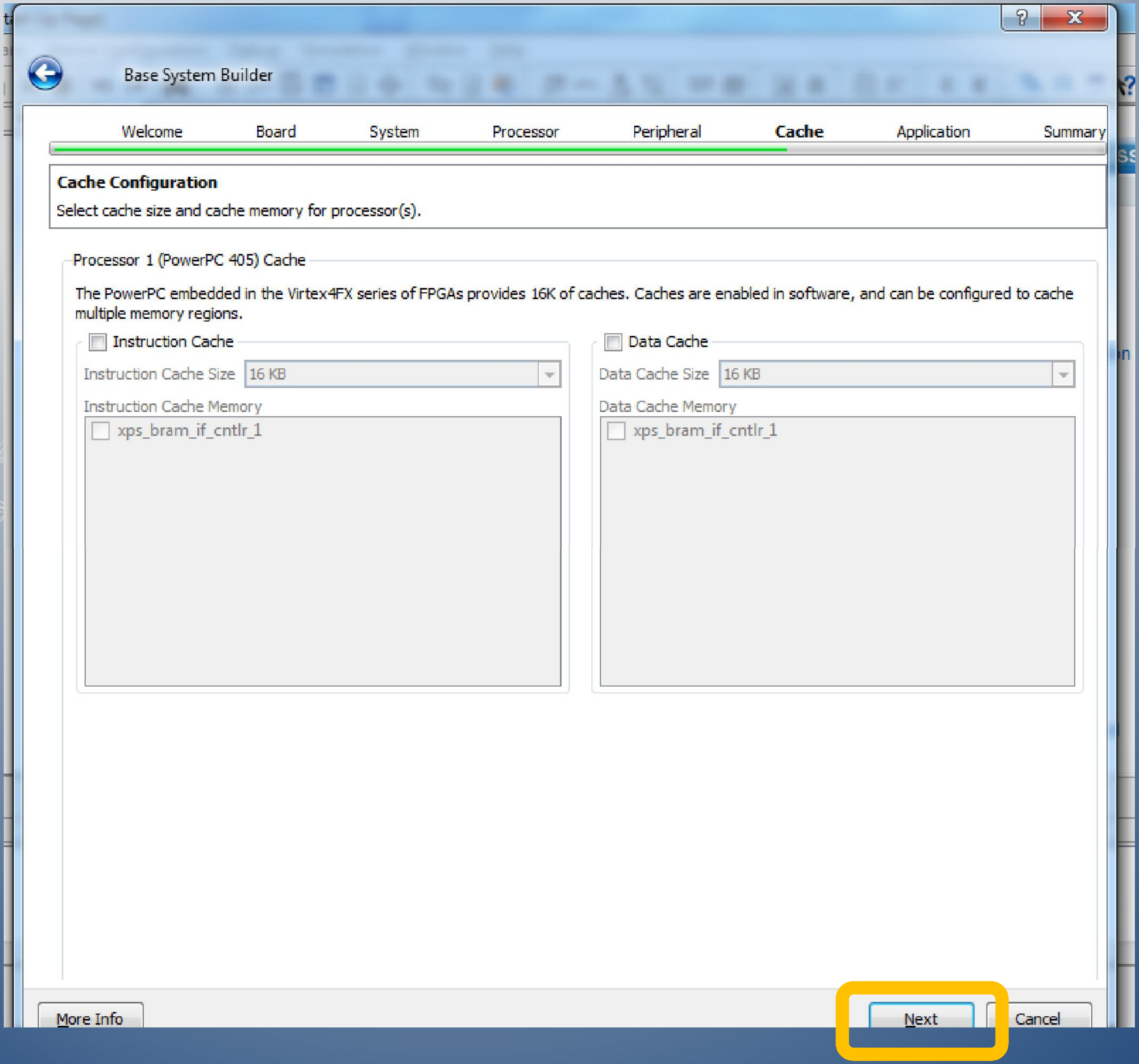
Processor 1 (PowerPC 405) Peripherals

Core	Parameter
DDR_SDRAM	
Core	
Ethernet_MAC	
Core: xps_ethernetlite	
IIC_EEPROM	
Core: xps_iic	
LEDs_4Bit	
Core: xps_gpio	
LEDs_Positions	
Core: xps_gpio	
MGT_wrapper	
Core: mgt_protector	
Push_Buttons_Position	
Core: xps_gpio	
RS232_Uart	
Core: xps_uartlite, Baud	
SRAM	
Core: xps_mch_emc	
SysACE_CompactFlash	
Core: xps_sysace	
xps_bram_if_cntlr_1	
Core: xps_bram_if_cntlr, Size: 8 KB	

Processor 1 (PowerPC 405) Peripherals

Core	Parameter
LEDs_4Bit	
Core: xps_gpio	
RS232_Uart	
Core: xps_uartlite, Baud Rate: 9600, Data ...	
xps_bram_if_cntlr_1	
Core: xps_bram_if_cntlr, Size: 8 KB	

Remove others than these three IPs



Cache Configuration

Select cache size and cache memory for processor(s).

Processor 1 (PowerPC 405) Cache

The PowerPC embedded in the Virtex4FX series of FPGAs provides 16K of caches. Caches are enabled in software, and can be configured to cache multiple memory regions.

☐ Instruction Cache

Instruction Cache Size: 16 KB

Instruction Cache Memory

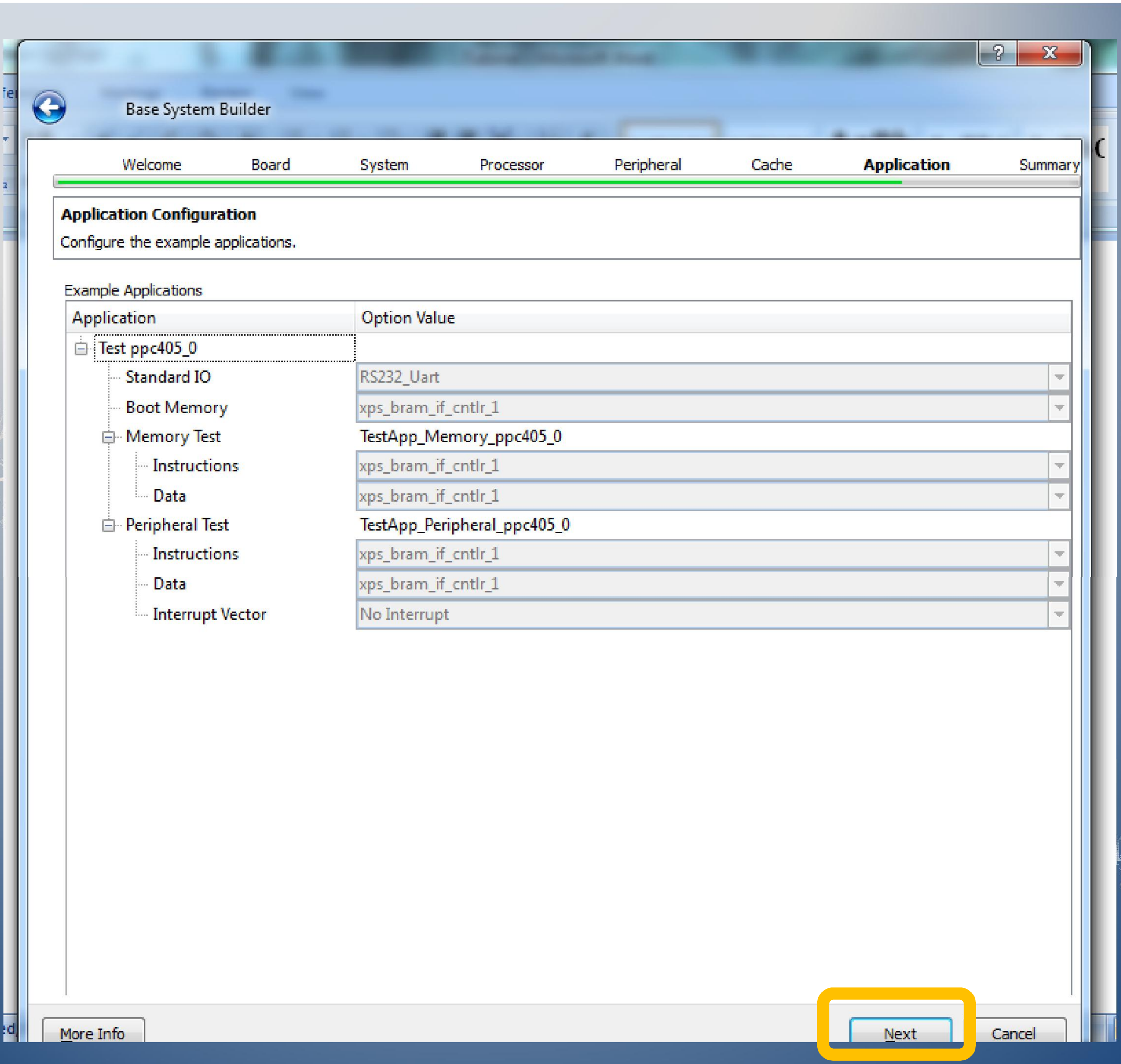
☐ xps_bram_if_cntlr_1

☐ Data Cache

Data Cache Size: 16 KB

Data Cache Memory

☐ xps_bram_if_cntlr_1

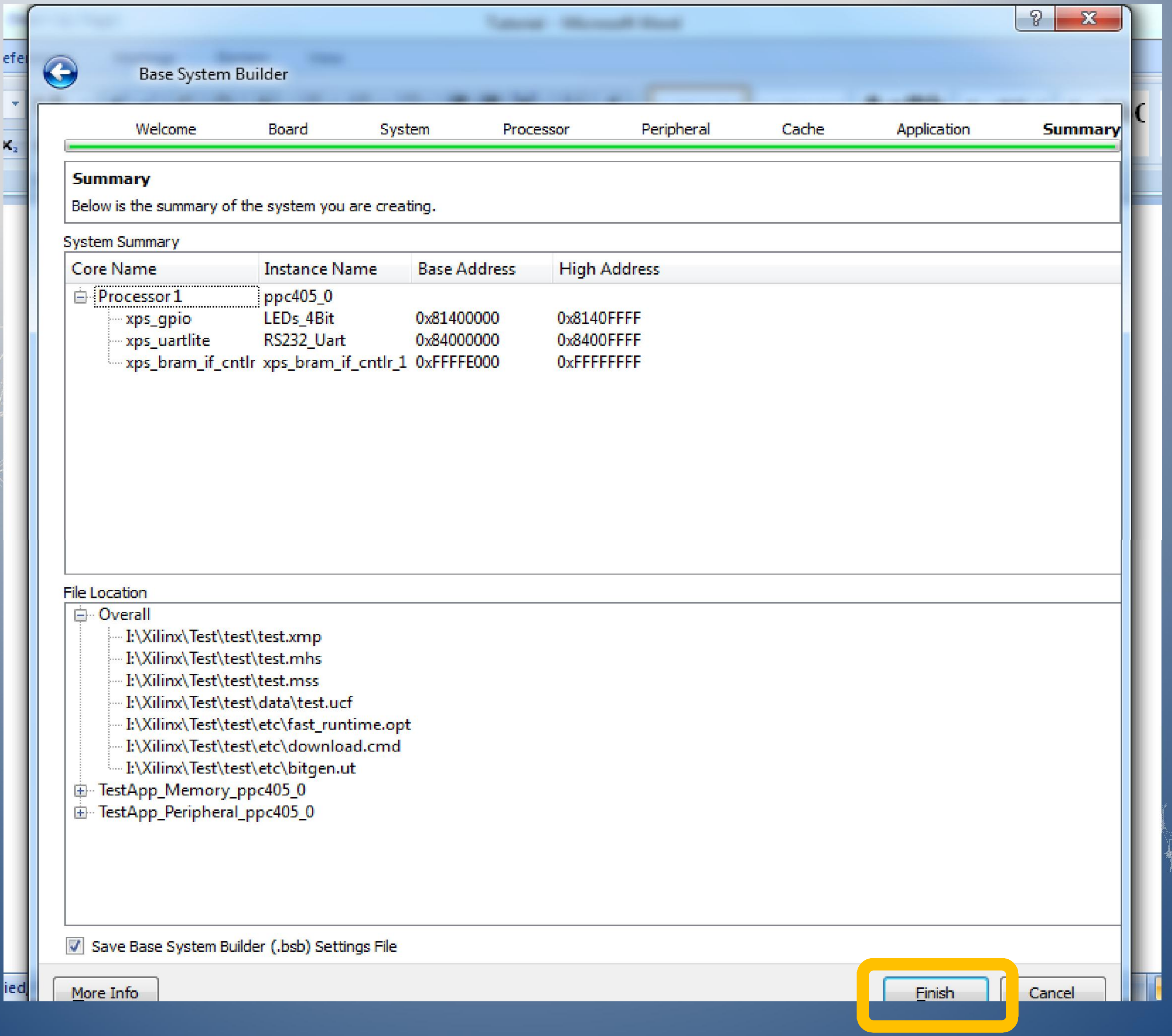


Application Configuration

Configure the example applications.

Example Applications

Application	Option Value
Test ppc405_0	
Standard IO	RS232_Uart
Boot Memory	xps_bram_if_cntlr_1
Memory Test	TestApp_Memory_ppc405_0
Instructions	xps_bram_if_cntlr_1
Data	xps_bram_if_cntlr_1
Peripheral Test	TestApp_Peripheral_ppc405_0
Instructions	xps_bram_if_cntlr_1
Data	xps_bram_if_cntlr_1
Interrupt Vector	No Interrupt



Summary

Below is the summary of the system you are creating.

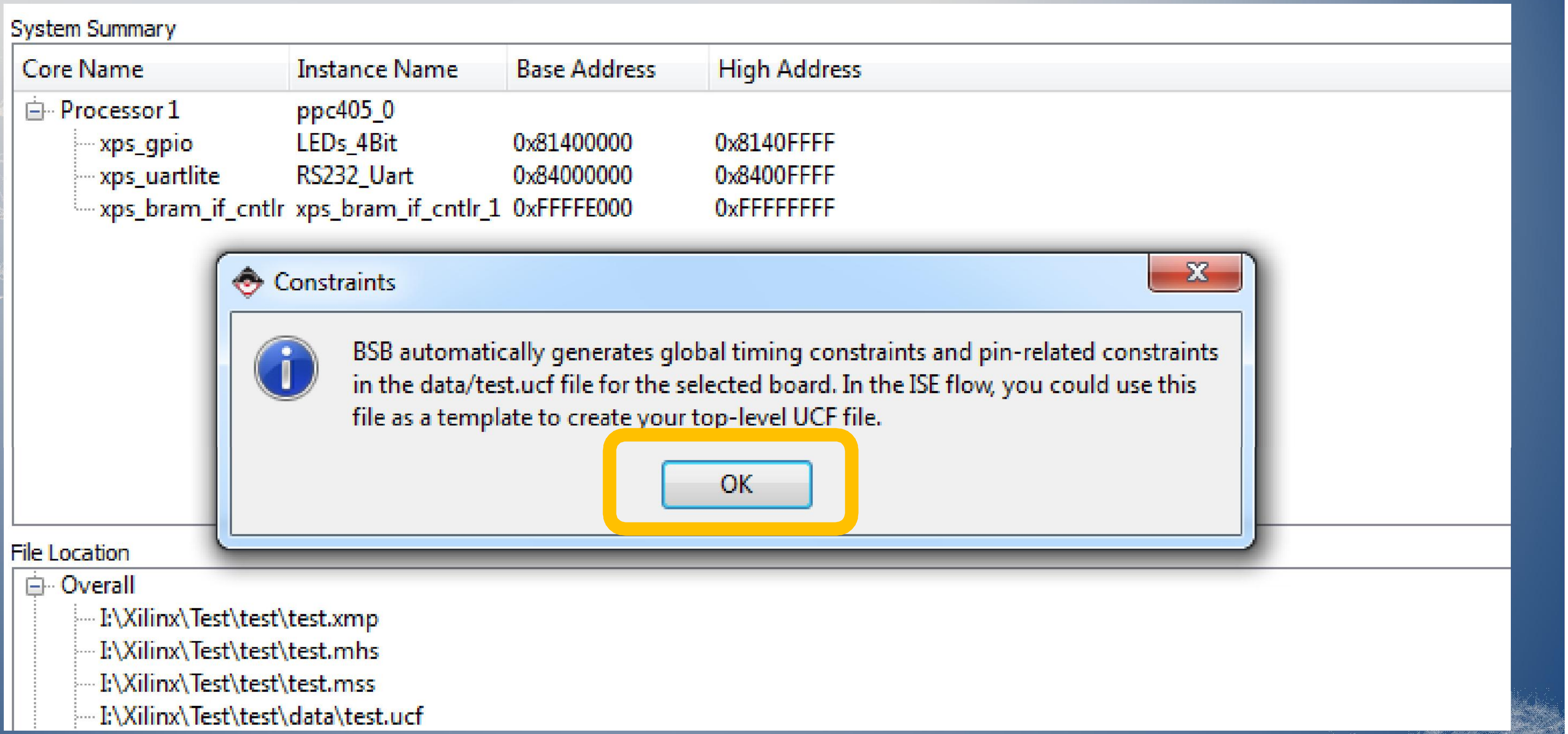
System Summary

Core Name	Instance Name	Base Address	High Address
⊟ Processor 1	ppc405_0		
xps_gpio	LEDs_4Bit	0x81400000	0x8140FFFF
xps_uartlite	RS232_Uart	0x84000000	0x8400FFFF
xps_bram_if_cntlr	xps_bram_if_cntlr_1	0xFFFFE000	0xFFFFFFFF

File Location

```
⊟ Overall
    I:\Xilinx\Test\test\test.xmp
    I:\Xilinx\Test\test\test.mhs
    I:\Xilinx\Test\test\test.mss
    I:\Xilinx\Test\test\data\test.ucf
    I:\Xilinx\Test\test\etc\fast_runtime.opt
    I:\Xilinx\Test\test\etc\download.cmd
    I:\Xilinx\Test\test\etc\bitgen.ut
⊞ TestApp_Memory_ppc405_0
⊞ TestApp_Peripheral_ppc405_0
```

☑ Save Base System Builder (.bsb) Settings File



System Summary

Core Name	Instance Name	Base Address	High Address
Processor 1	ppc405_0		
xps_gpio	LEDs_4Bit	0x81400000	0x8140FFFF
xps_uartlite	RS232_Uart	0x84000000	0x8400FFFF
xps_bram_if_cntlr	xps_bram_if_cntlr_1	0xFFFFE000	0xFFFFFFFF

Constraints

BSB automatically generates global timing constraints and pin-related constraints in the data/test.ucf file for the selected board. In the ISE flow, you could use this file as a template to create your top-level UCF file.

File Location

Overall

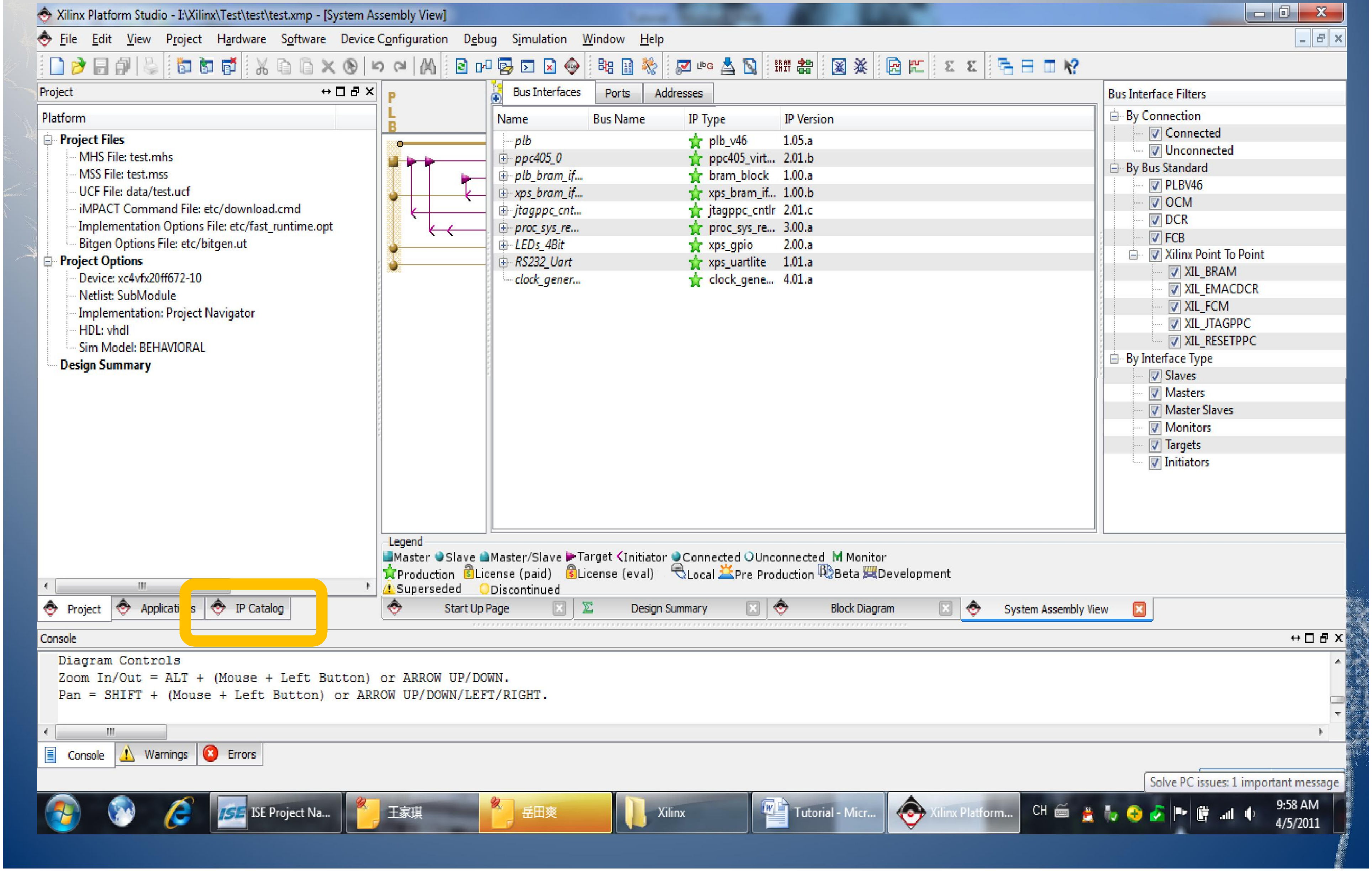
I:\Xilinx\Test\test\test.xmp

I:\Xilinx\Test\test\test.mhs

I:\Xilinx\Test\test\test.mss

I:\Xilinx\Test\test\data\test.ucf

Add IP Cores



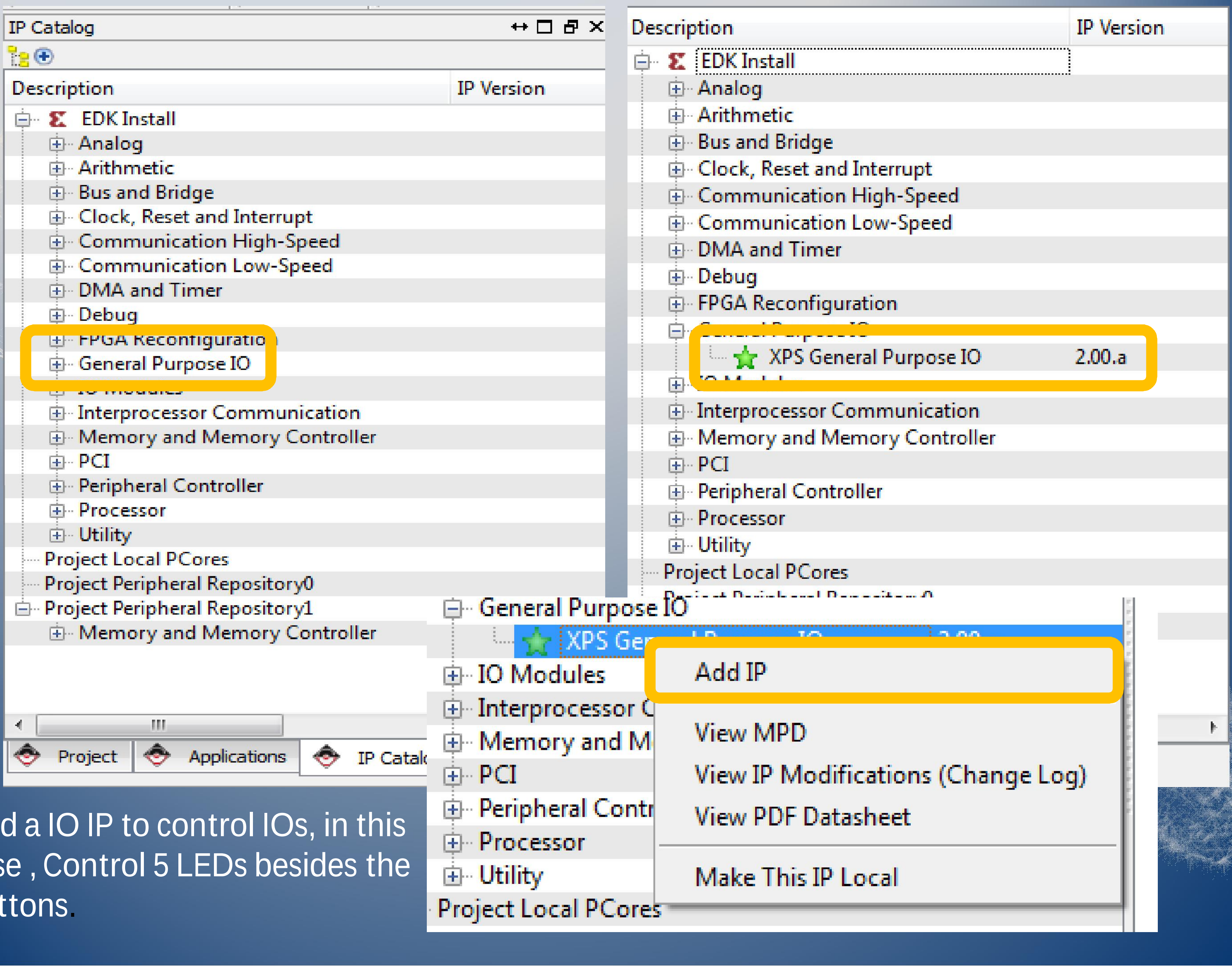
- Project Files
  - MHS File: test.mhs
  - MSS File: test.mss
  - UCF File: data/test.ucf
  - iMPACT Command File: etc/download.cmd
  - Implementation Options File: etc/fast_runtime.opt
  - Bitgen Options File: etc/bitgen.ut
- Project Options
  - Device: xc4vfx20ff672-10
  - Netlist: SubModule
  - Implementation: Project Navigator
  - HDL: vhdl
  - Sim Model: BEHAVIORAL
- Design Summary

Name	Bus Name	IP Type	IP Version
plb		plb_v46	1.05.a
ppc405_0		ppc405_virt...	2.01.b
plb_bram_if...		bram_block	1.00.a
xps_bram_if...		xps_bram_if...	1.00.b
jtagppc_cnt...		jtagppc_cntlr	2.01.c
proc_sys_re...		proc_sys_re...	3.00.a
LEDs_4Bit		xps_gpio	2.00.a
RS232_Uart		xps_uartlite	1.01.a
clock_gener...		clock_gene...	4.01.a

- By Connection
  - ☑ Connected
  - ☑ Unconnected
- By Bus Standard
  - ☑ PLBV46
  - ☑ OCM
  - ☑ DCR
  - ☑ FCB
  - ☑ Xilinx Point To Point
    - ☑ XIL_BRAM
    - ☑ XIL_EMACDCR
    - ☑ XIL_FCM
    - ☑ XIL_JTAGPPC
    - ☑ XIL_RESETPPC
- By Interface Type
  - ☑ Slaves
  - ☑ Masters
  - ☑ Master Slaves
  - ☑ Monitors
  - ☑ Targets
  - ☑ Initiators

Legend
Master Slave Master/Slave Target Initiator Connected Unconnected Monitor
Production License (paid) License (eval) Local Pre Production Beta Development
Superseded Discontinued

```
Diagram Controls
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
```

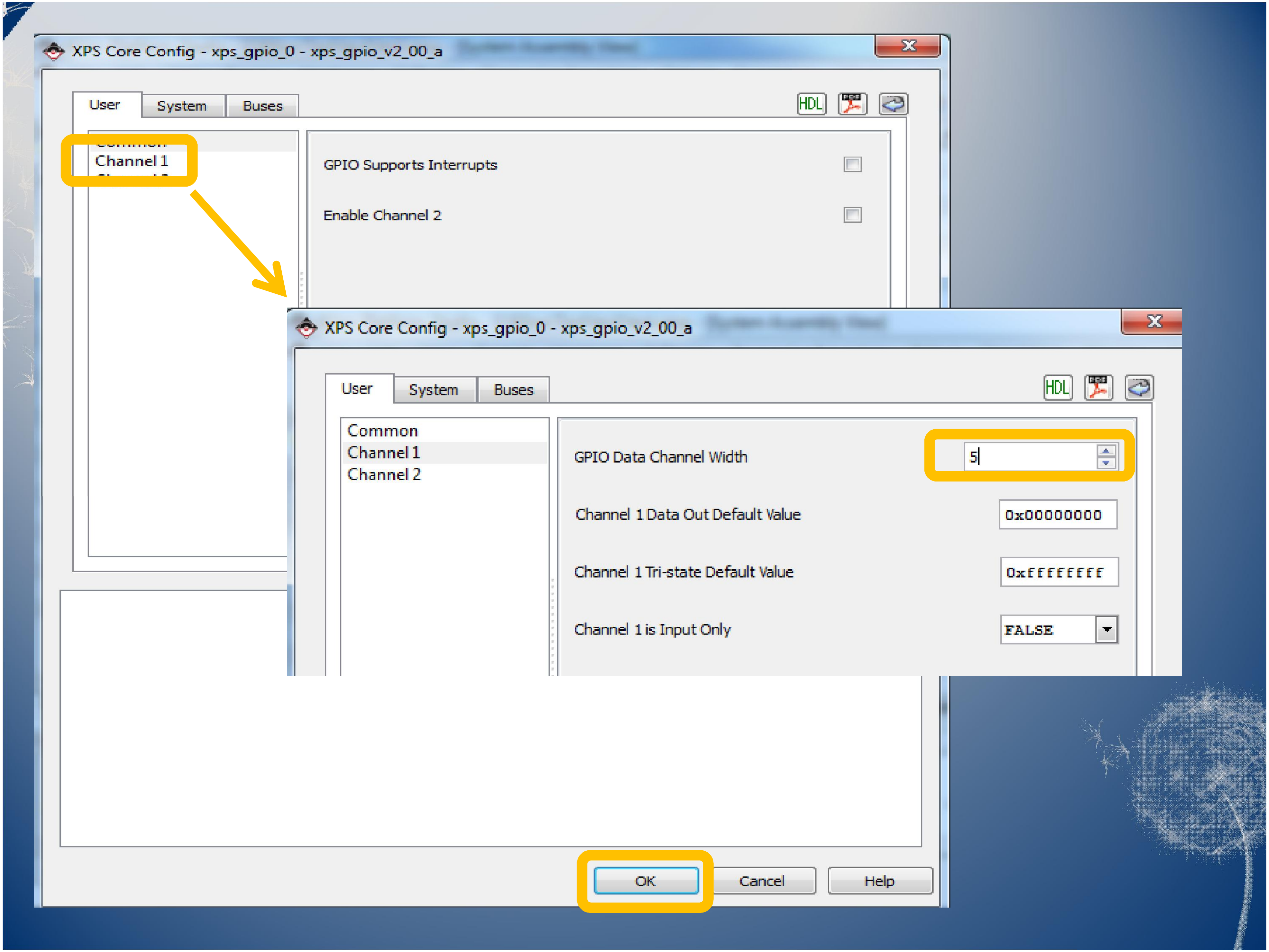


IP Catalog

Description	IP Version
EDK Install	
Analog	
Arithmetic	
Bus and Bridge	
Clock, Reset and Interrupt	
Communication High-Speed	
Communication Low-Speed	
DMA and Timer	
Debug	
FPGA Reconfiguration	
General Purpose IO	
IO Modules	
Interprocessor Communication	
Memory and Memory Controller	
PCI	
Peripheral Controller	
Processor	
Utility	
Project Local PCores	
Project Peripheral Repository0	
Project Peripheral Repository1	
Memory and Memory Controller	

Description	IP Version
EDK Install	
Analog	
Arithmetic	
Bus and Bridge	
Clock, Reset and Interrupt	
Communication High-Speed	
Communication Low-Speed	
DMA and Timer	
Debug	
FPGA Reconfiguration	
General Purpose IO	
XPS General Purpose IO	2.00.a
IO Modules	
Interprocessor Communication	
Memory and Memory Controller	
PCI	
Peripheral Controller	
Processor	
Utility	
Project Local PCores	
Project Peripheral Repository0	

Add a IO IP to control IOs, in this case , Control 5 LEDs besides the buttons.



GPIO Supports Interrupts ☐

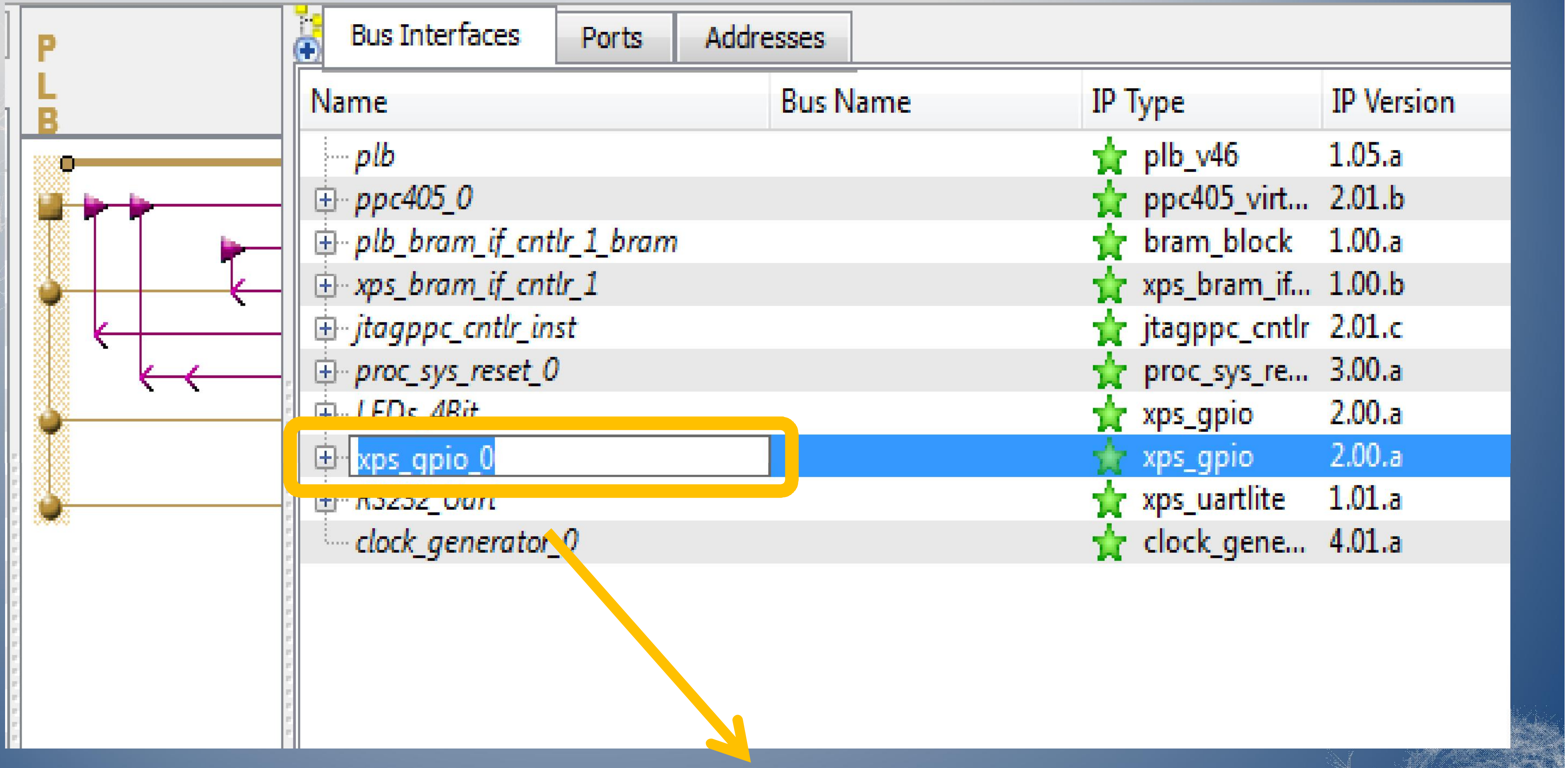
Enable Channel 2 ☐

GPIO Data Channel Width: 5

Channel 1 Data Out Default Value: 0x00000000

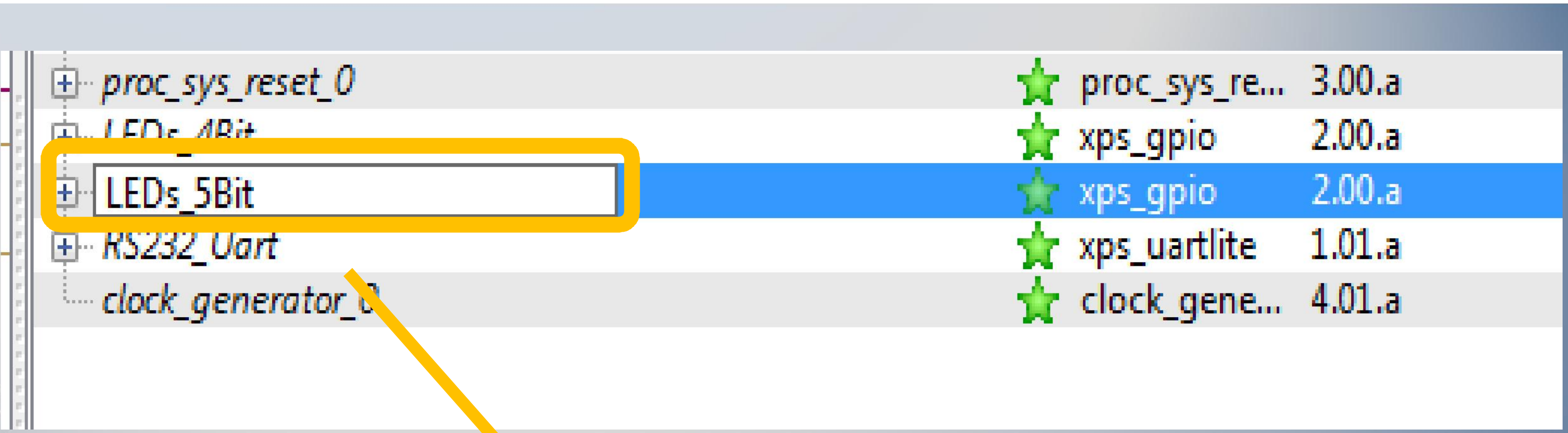
Channel 1 Tri-state Default Value: 0xffffffff

Channel 1 is Input Only: FALSE



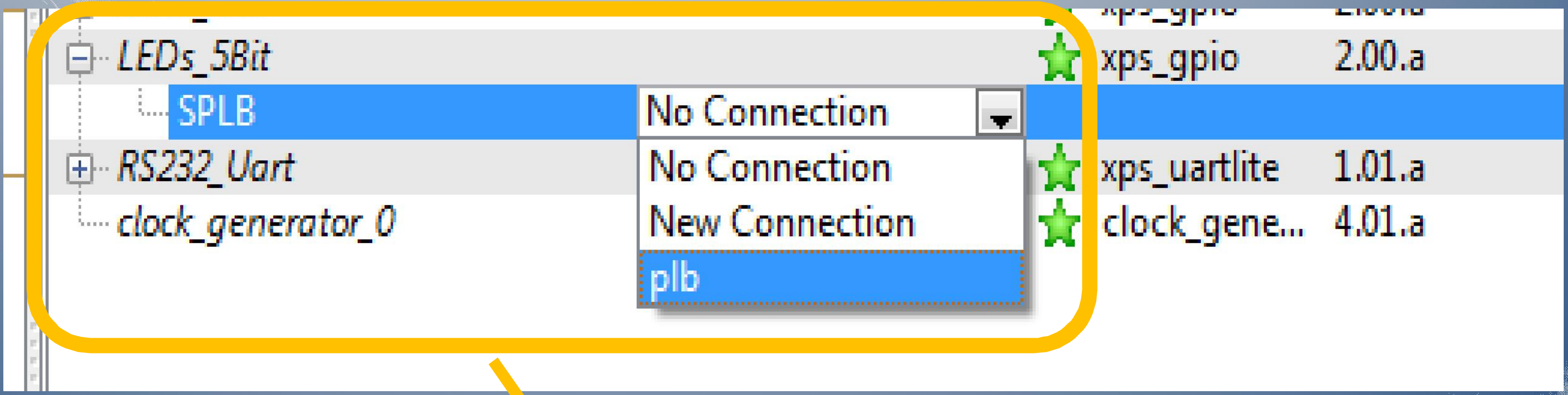
Name	Bus Name	IP Type	IP Version
plb		plb_v46	1.05.a
ppc405_0		ppc405_virt...	2.01.b
plb_bram_if_cntlr_1_bram		bram_block	1.00.a
xps_bram_if_cntlr_1		xps_bram_if...	1.00.b
jtagppc_cntlr_inst		jtagppc_cntlr	2.01.c
proc_sys_reset_0		proc_sys_re...	3.00.a
LEDs_4Bit		xps_gpio	2.00.a
xps_gpio_0		xps_gpio	2.00.a
RS232_Uart		xps_uartlite	1.01.a
clock_generator_0		clock_gene...	4.01.a

Change the name by click once on the name.



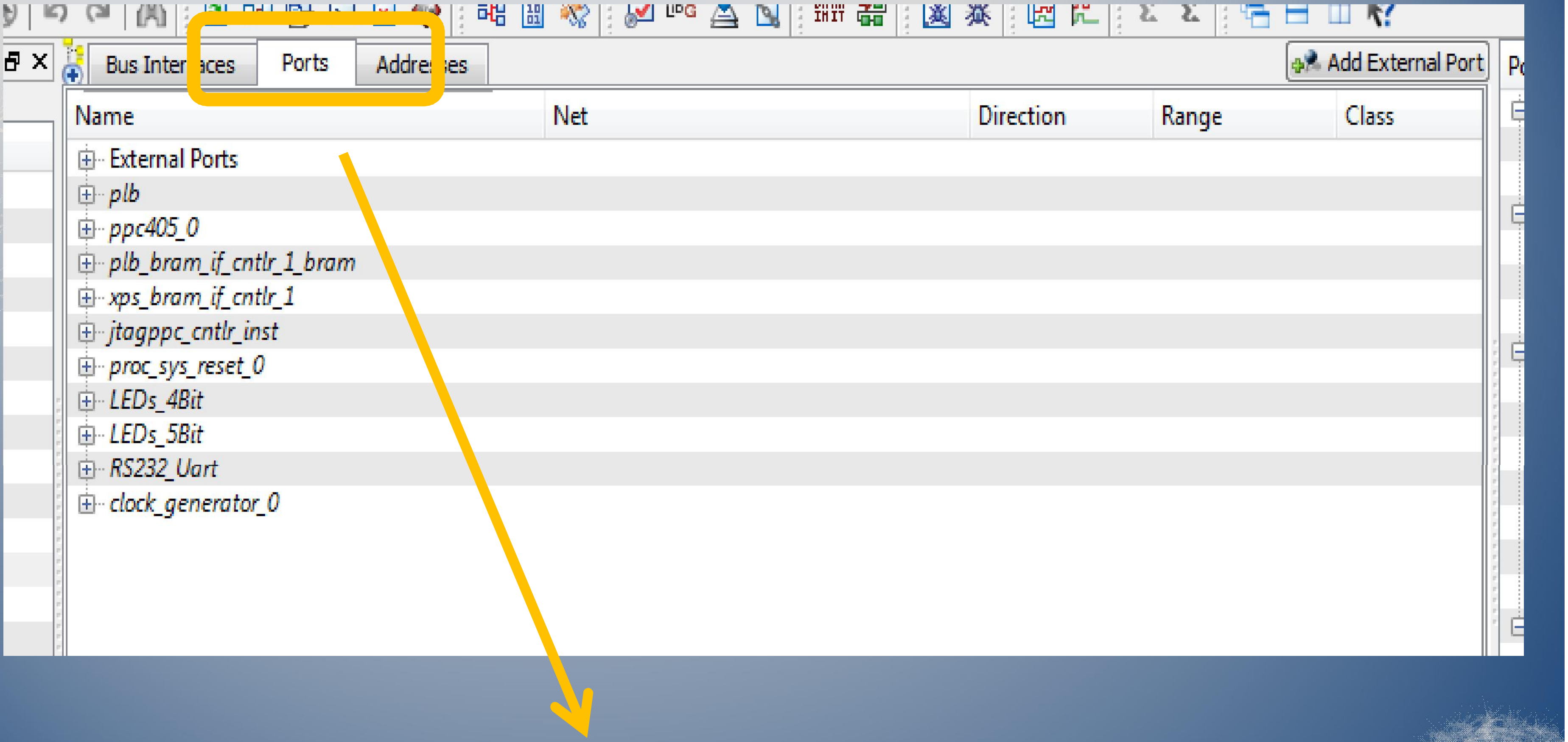
proc_sys_reset_0	proc_sys_re...	3.00.a
LEDs_4Bit	xps_gpio	2.00.a
LEDs_5Bit	xps_gpio	2.00.a
RS232_Uart	xps_uartlite	1.01.a
clock_generator_0	clock_gene...	4.01.a

Change the name to LEDs_5Bit



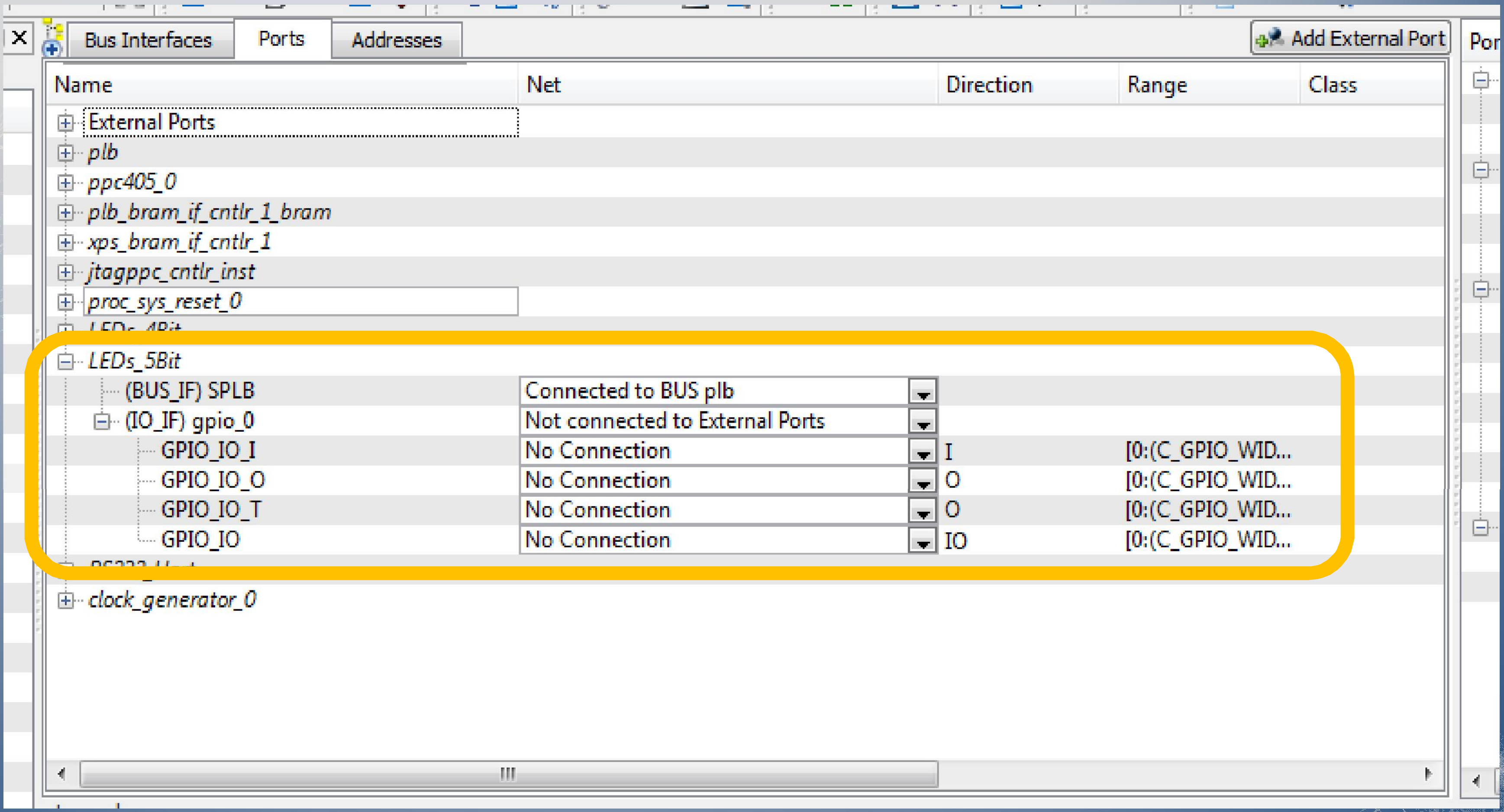
LEDs_5Bit	xps_gpio	2.00.a
SPLB	No Connection	
RS232_Uart	xps_uartlite	1.01.a
clock_generator_0	clock_gene...	4.01.a

Connect it to plb bus

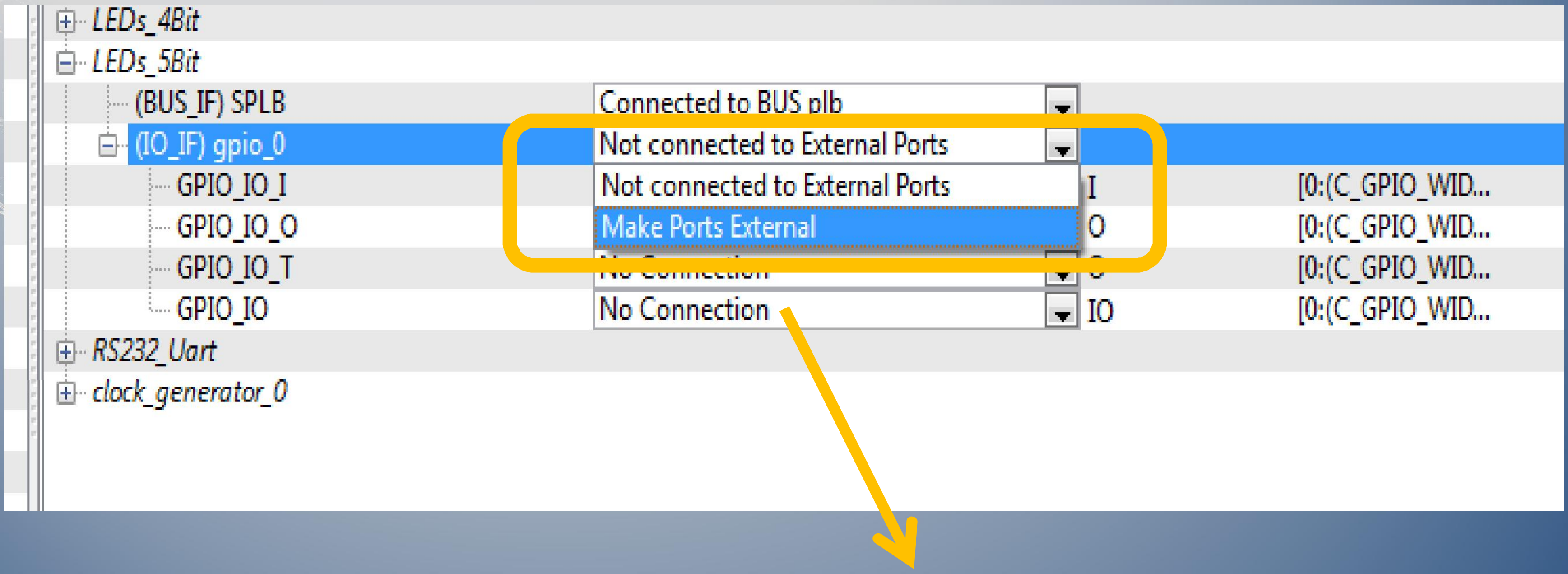


Name	Net	Direction	Range	Class
External Ports				
plb				
ppc405_0				
plb_bram_if_cntlr_1_bram				
xps_bram_if_cntlr_1				
jtagppc_cntlr_inst				
proc_sys_reset_0				
LEDs_4Bit				
LEDs_5Bit				
RS232_Uart				
clock_generator_0				

Connect IP core’s ports

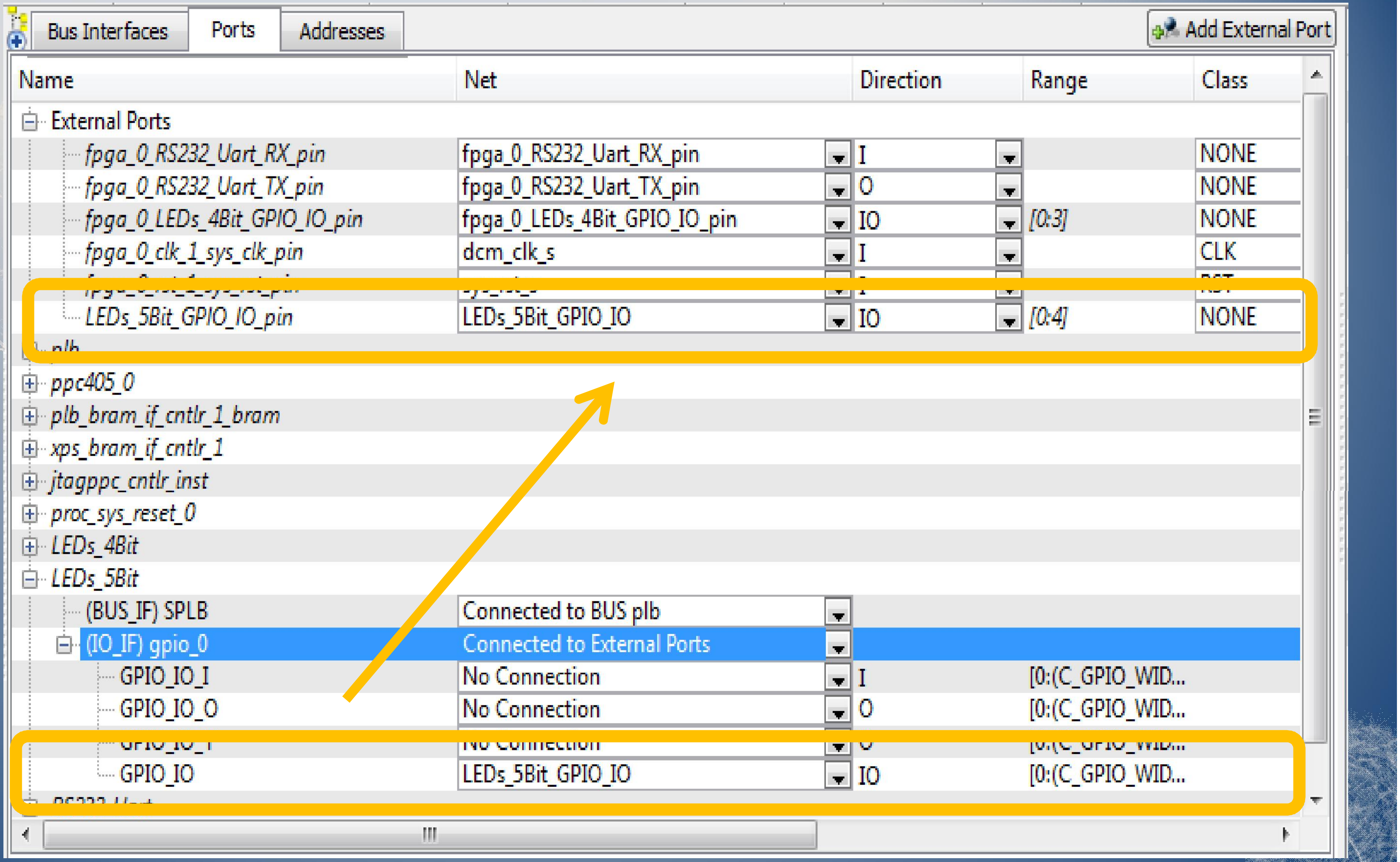


Name	Net	Direction	Range	Class
External Ports				
plb				
ppc405_0				
plb_bram_if_cntlr_1_bram				
xps_bram_if_cntlr_1				
jtagppc_cntlr_inst				
proc_sys_reset_0				
LEDs_4Bit				
LEDs_5Bit				
(BUS_IF) SPLB	Connected to BUS plb			
(IO_IF) gpio_0	Not connected to External Ports			
GPIO_IO_I	No Connection	I	[0:(C_GPIO_WID...	
GPIO_IO_O	No Connection	O	[0:(C_GPIO_WID...	
GPIO_IO_T	No Connection	O	[0:(C_GPIO_WID...	
GPIO_IO	No Connection	IO	[0:(C_GPIO_WID...	
RS232_Uart				
clock_generator_0				



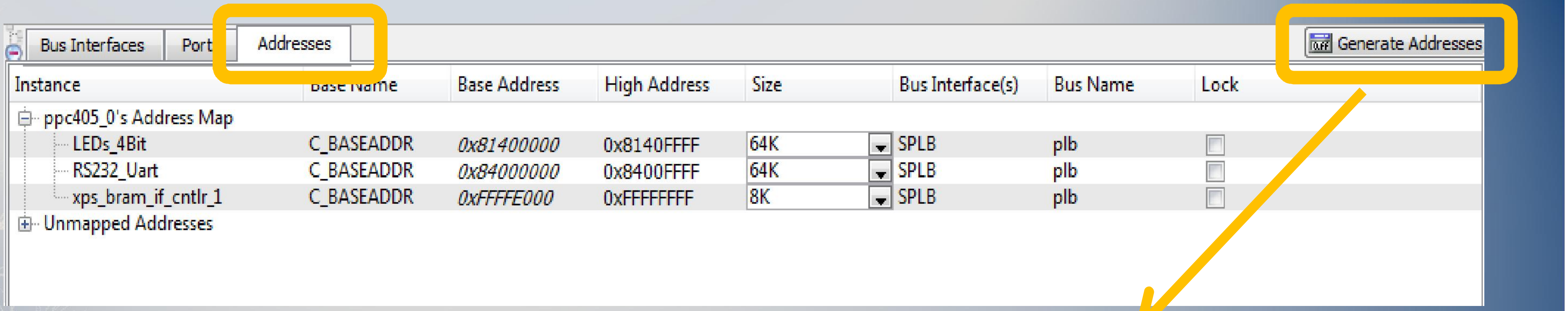
LEDs_4Bit			
LEDs_5Bit			
(BUS_IF) SPLB	Connected to BUS plb		
(IO_IF) gpio_0	Not connected to External Ports		
GPIO_IO_I		I	[0:(C_GPIO_WID...
GPIO_IO_O		O	[0:(C_GPIO_WID...
GPIO_IO_T	No Connection	O	[0:(C_GPIO_WID...
GPIO_IO	No Connection	IO	[0:(C_GPIO_WID...
RS232_Uart			
clock_generator_0			

Connect its ports to external ports



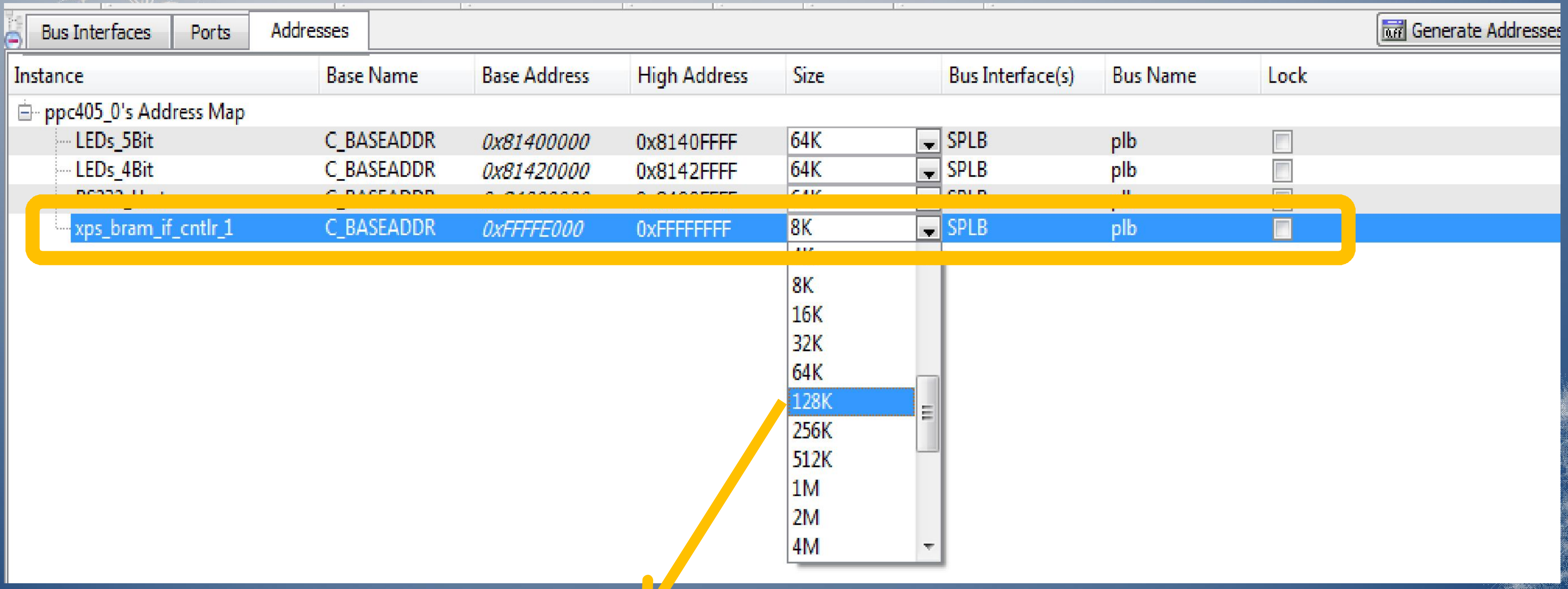
Name	Net	Direction	Range	Class
External Ports				
fpga_0_RS232_Uart_RX_pin	fpga_0_RS232_Uart_RX_pin	I		NONE
fpga_0_RS232_Uart_TX_pin	fpga_0_RS232_Uart_TX_pin	O		NONE
fpga_0_LEDs_4Bit_GPIO_IO_pin	fpga_0_LEDs_4Bit_GPIO_IO_pin	IO	*[0:3]*	NONE
fpga_0_clk_1_sys_clk_pin	dcm_clk_s	I		CLK
fpga_0_rst_1_sys_rst_pin	sys_rst_s	I		RST
LEDs_5Bit_GPIO_IO_pin	LEDs_5Bit_GPIO_IO	IO	*[0:4]*	NONE
plb				
ppc405_0				
plb_bram_if_cntlr_1_bram				
xps_bram_if_cntlr_1				
jtagppc_cntlr_inst				
proc_sys_reset_0				
LEDs_4Bit				
LEDs_5Bit				
(BUS_IF) SPLB	Connected to BUS plb			
(IO_IF) gpio_0	Connected to External Ports			
GPIO_IO_I	No Connection	I	[0:(C_GPIO_WID...	
GPIO_IO_O	No Connection	O	[0:(C_GPIO_WID...	
GPIO_IO_T	No Connection	O	[0:(C_GPIO_WID...	
GPIO_IO	LEDs_5Bit_GPIO_IO	IO	[0:(C_GPIO_WID...	
RS232_Uart				

Check External Ports, they are connected automatically.



Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
ppc405_0's Address Map							
LEDs_4Bit	C_BASEADDR	*0x81400000*	0x8140FFFF	64K	SPLB	plb	□
RS232_Uart	C_BASEADDR	*0x84000000*	0x8400FFFF	64K	SPLB	plb	□
xps_bram_if_cntlr_1	C_BASEADDR	*0xFFFFE000*	0xFFFFFFFF	8K	SPLB	plb	□
Unmapped Addresses							

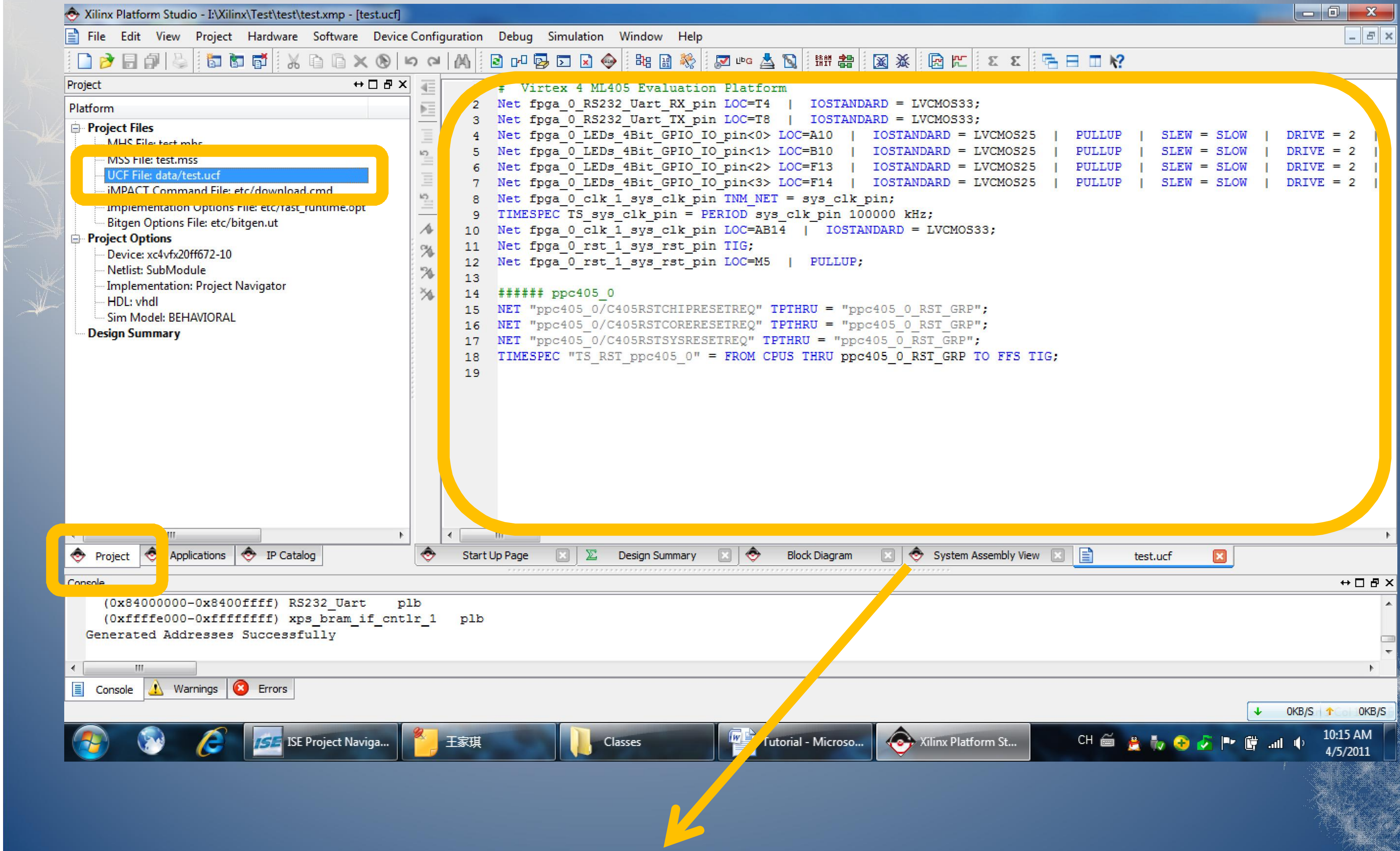
Click and Generate addresses for IPs automatically



Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
ppc405_0's Address Map							
LEDs_5Bit	C_BASEADDR	*0x81400000*	0x8140FFFF	64K	SPLB	plb	□
LEDs_4Bit	C_BASEADDR	*0x81420000*	0x8142FFFF	64K	SPLB	plb	□
[illegible]	C_BASEADDR	[illegible]	[illegible]	64K	SPLB	plb	□
xps_bram_if_cntlr_1	C_BASEADDR	*0xFFFFE000*	0xFFFFFFFF	8K	SPLB	plb	□

Change this IP’s size

Edit the UCF file to assign FPGA's PINs to IP's Ports



Xilinx Platform Studio - I:\Xilinx\Test\test\test.xmp - [test.ucf]

Project

Platform

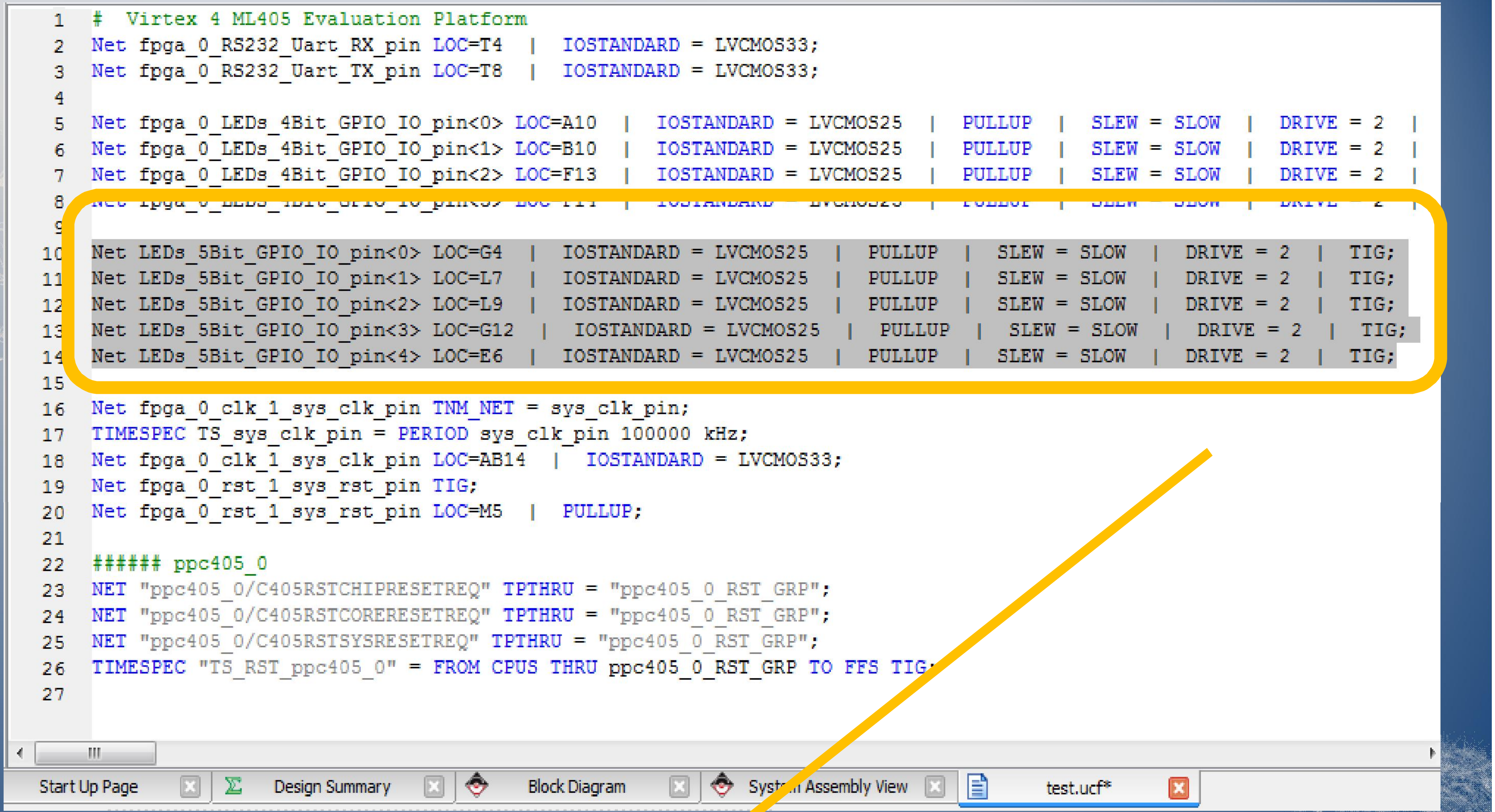
- Project Files
  - MHS File: test.mhs
  - MSS File: test.mss
  - UCF File: data/test.ucf
  - iMPACT Command File: etc/download.cmd
  - Implementation Options File: etc/fast_runtime.opt
  - Bitgen Options File: etc/bitgen.ut
- Project Options
  - Device: xc4vfx20ff672-10
  - Netlist: SubModule
  - Implementation: Project Navigator
  - HDL: vhdl
  - Sim Model: BEHAVIORAL
- Design Summary

```
#  Virtex 4 ML405 Evaluation Platform
Net fpga_0_RS232_Uart_RX_pin LOC=T4  |  IOSTANDARD = LVCMOS33;
Net fpga_0_RS232_Uart_TX_pin LOC=T8  |  IOSTANDARD = LVCMOS33;
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<0> LOC=A10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<1> LOC=B10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<2> LOC=F13  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<3> LOC=F14  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_clk_1_sys_clk_pin TNM_NET = sys_clk_pin;
TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 100000 kHz;
Net fpga_0_clk_1_sys_clk_pin LOC=AB14  |  IOSTANDARD = LVCMOS33;
Net fpga_0_rst_1_sys_rst_pin TIG;
Net fpga_0_rst_1_sys_rst_pin LOC=M5  |  PULLUP;

###### ppc405_0
NET "ppc405_0/C405RSTCHIPRESETREQ" TPTHRU = "ppc405_0_RST_GRP";
NET "ppc405_0/C405RSTCORERESETREQ" TPTHRU = "ppc405_0_RST_GRP";
NET "ppc405_0/C405RSTSYSRESETREQ" TPTHRU = "ppc405_0_RST_GRP";
TIMESPEC "TS_RST_ppc405_0" = FROM CPUS THRU ppc405_0_RST_GRP TO FFS TIG;
```

Console

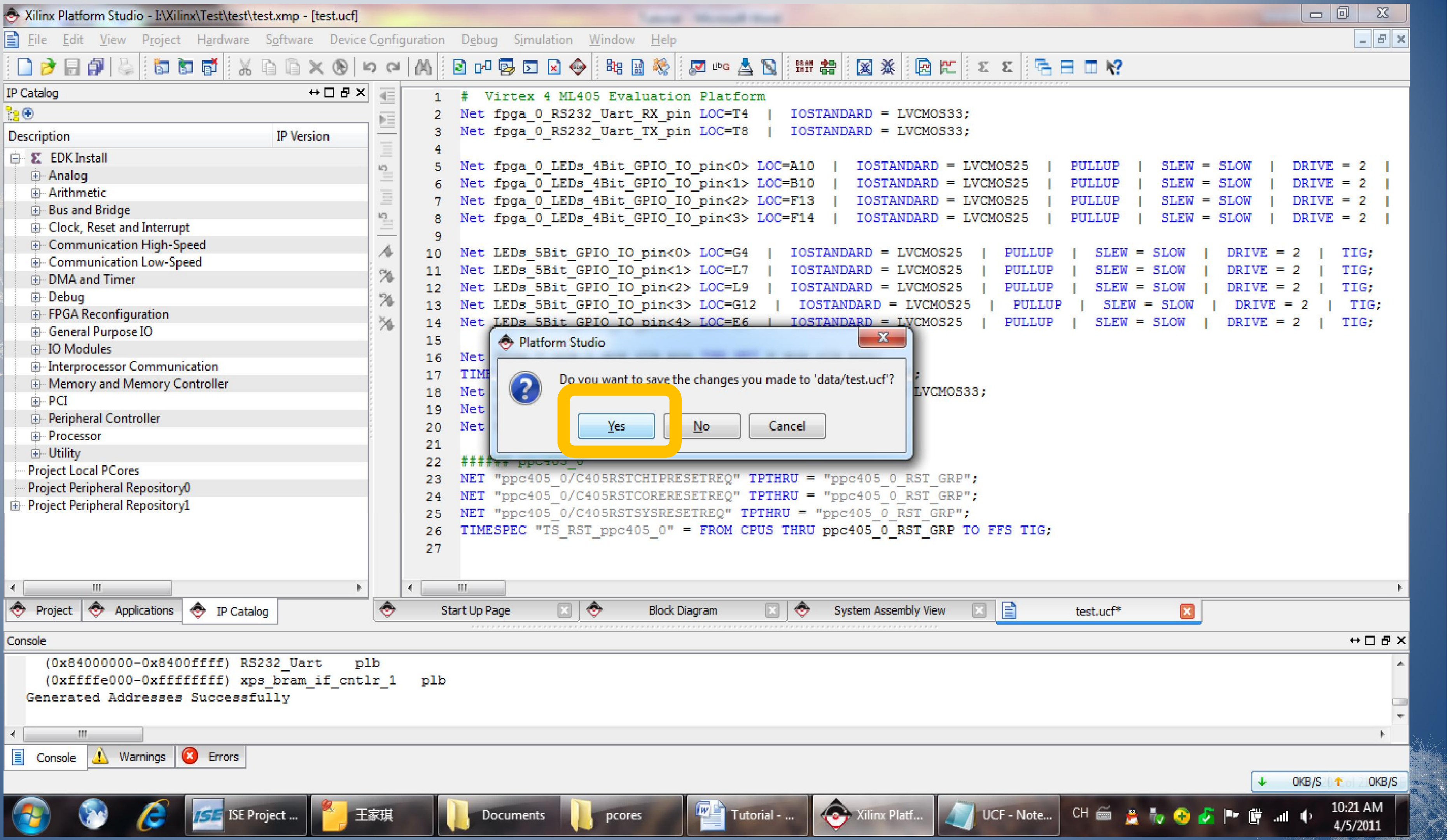
```
   (0x84000000-0x8400ffff) RS232_Uart    plb
   (0xffffe000-0xffffffff) xps_bram_if_cntlr_1   plb
Generated Addresses Successfully
```

UCF file



```
#  Virtex 4 ML405 Evaluation Platform
Net fpga_0_RS232_Uart_RX_pin LOC=T4  |  IOSTANDARD = LVCMOS33;
Net fpga_0_RS232_Uart_TX_pin LOC=T8  |  IOSTANDARD = LVCMOS33;

Net fpga_0_LEDs_4Bit_GPIO_IO_pin<0> LOC=A10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<1> LOC=B10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<2> LOC=F13  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<3> LOC=F14  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |

Net LEDs_5Bit_GPIO_IO_pin<0> LOC=G4  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<1> LOC=L7  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;

Net fpga_0_clk_1_sys_clk_pin TNM_NET = sys_clk_pin;
TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 100000 kHz;
Net fpga_0_clk_1_sys_clk_pin LOC=AB14  |  IOSTANDARD = LVCMOS33;
Net fpga_0_rst_1_sys_rst_pin TIG;
Net fpga_0_rst_1_sys_rst_pin LOC=M5  |  PULLUP;

###### ppc405_0
NET "ppc405_0/C405RSTCHIPRESETREQ" TPTHRU = "ppc405_0_RST_GRP";
NET "ppc405_0/C405RSTCORERESETREQ" TPTHRU = "ppc405_0_RST_GRP";
NET "ppc405_0/C405RSTSYSRESETREQ" TPTHRU = "ppc405_0_RST_GRP";
TIMESPEC "TS_RST_ppc405_0" = FROM CPUS THRU ppc405_0_RST_GRP TO FFS TIG;
```

Copy these from the UCF text document
in the “Documents” folder



```
#  Virtex 4 ML405 Evaluation Platform
Net fpga_0_RS232_Uart_RX_pin LOC=T4  |  IOSTANDARD = LVCMOS33;
Net fpga_0_RS232_Uart_TX_pin LOC=T8  |  IOSTANDARD = LVCMOS33;

Net fpga_0_LEDs_4Bit_GPIO_IO_pin<0> LOC=A10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<1> LOC=B10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<2> LOC=F13  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<3> LOC=F14  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |

Net LEDs_5Bit_GPIO_IO_pin<0> LOC=G4  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<1> LOC=L7  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;

Net
TIM                                                  ;
Net                                                  LVCMOS33;
Net
Net

###### ppc405_0
NET "ppc405_0/C405RSTCHIPRESETREQ" TPTHRU = "ppc405_0_RST_GRP";
NET "ppc405_0/C405RSTCORERESETREQ" TPTHRU = "ppc405_0_RST_GRP";
NET "ppc405_0/C405RSTSYSRESETREQ" TPTHRU = "ppc405_0_RST_GRP";
TIMESPEC "TS_RST_ppc405_0" = FROM CPUS THRU ppc405_0_RST_GRP TO FFS TIG;
```

Platform Studio

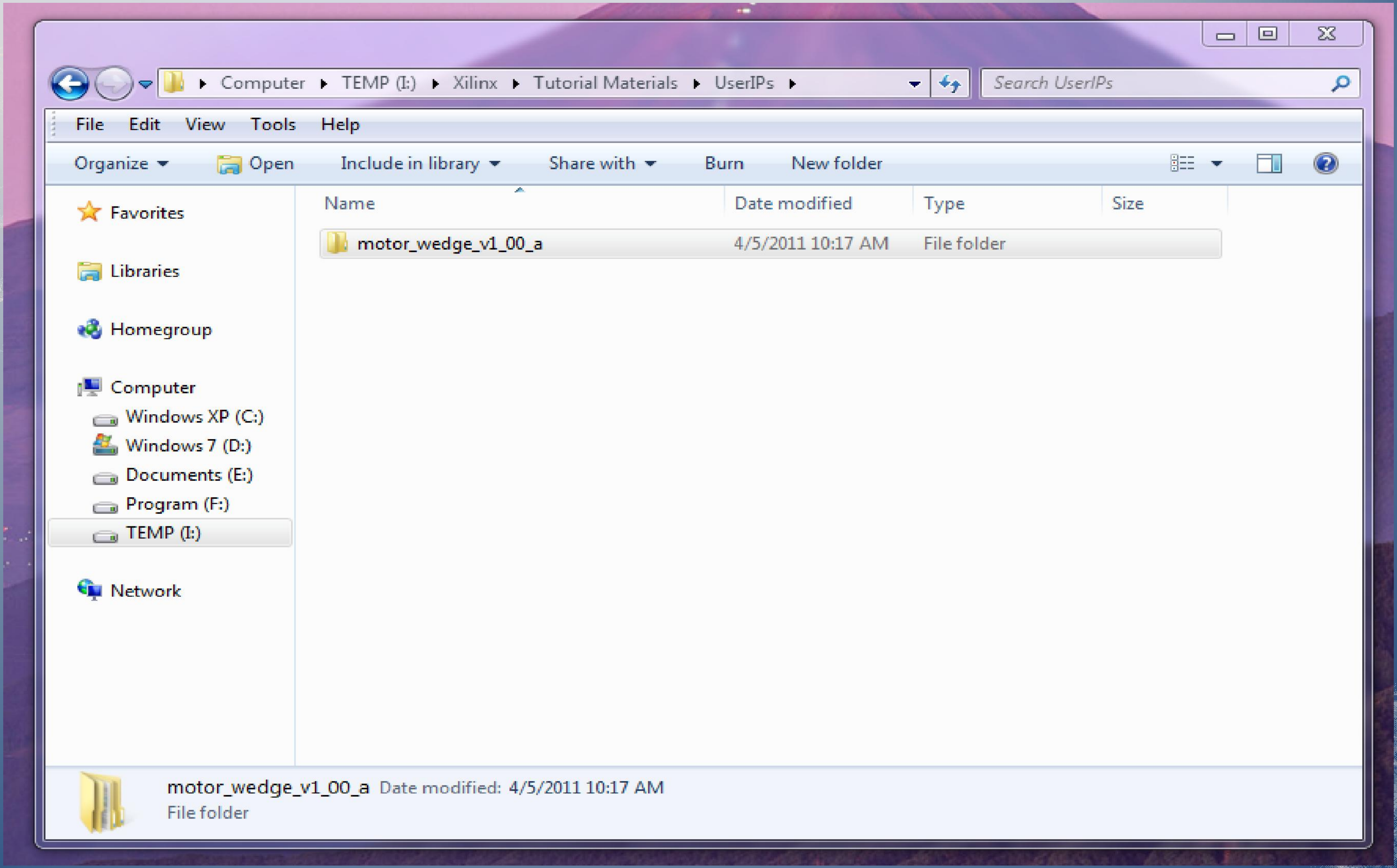
Do you want to save the changes you made to 'data/test.ucf'?

Yes No Cancel

```
    (0x84000000-0x8400ffff) RS232_Uart     plb
    (0xffffe000-0xffffffff) xps_bram_if_cntlr_1    plb
Generated Addresses Successfully
```

Save the file and close XPS, because next step we are going to add a custom IP core

Add a custom IP Cores

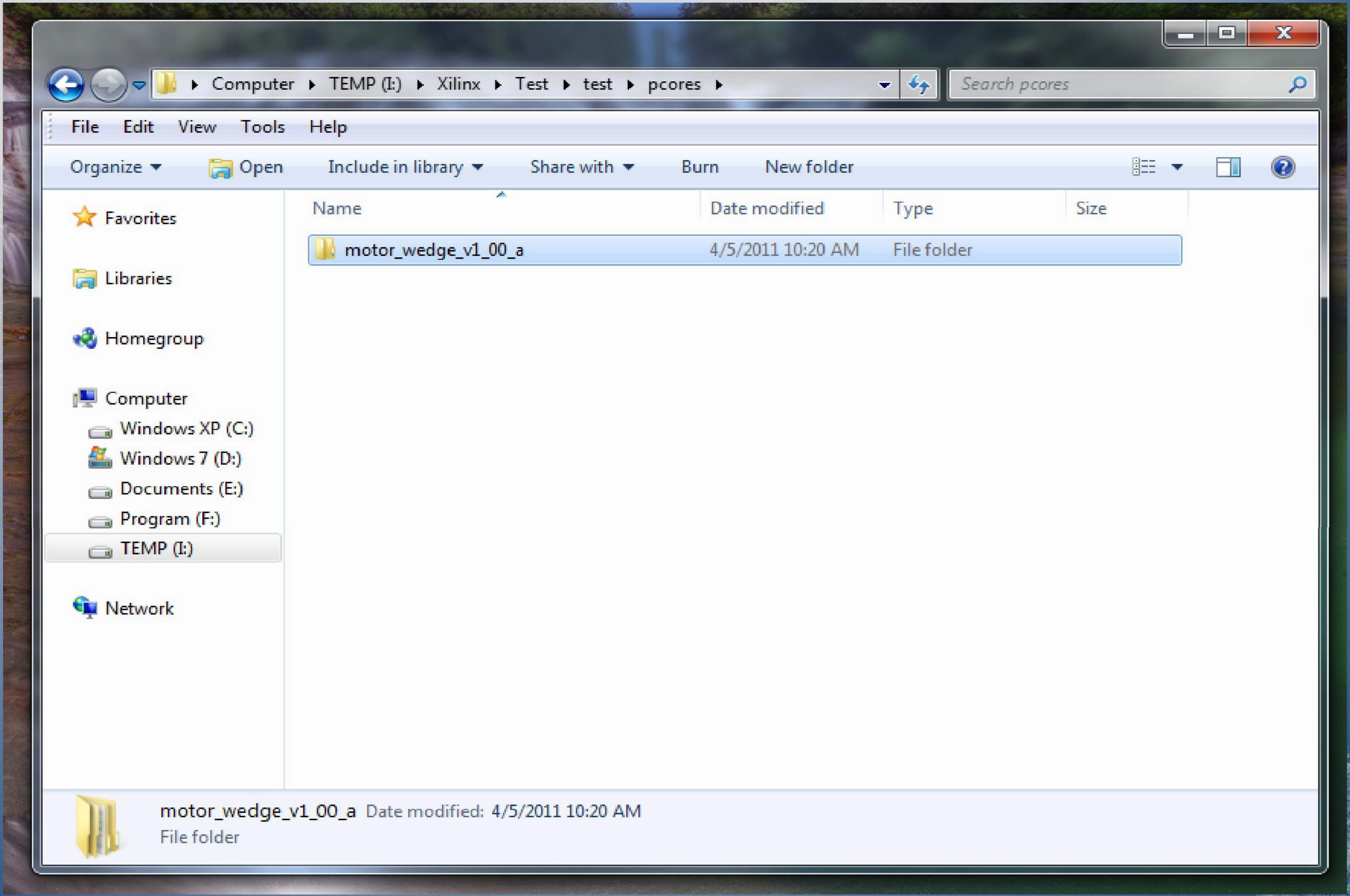


Computer ▸ TEMP (I:) ▸ Xilinx ▸ Tutorial Materials ▸ UserIPs ▸
Search UserIPs
File Edit View Tools Help
Organize ▾ Open Include in library ▾ Share with ▾ Burn New folder
Favorites
Libraries
Homegroup
Computer
Windows XP (C:)
Windows 7 (D:)
Documents (E:)
Program (F:)
TEMP (I:)
Network

Name	Date modified	Type	Size
motor_wedge_v1_00_a	4/5/2011 10:17 AM	File folder	

motor_wedge_v1_00_a Date modified: 4/5/2011 10:17 AM
File folder

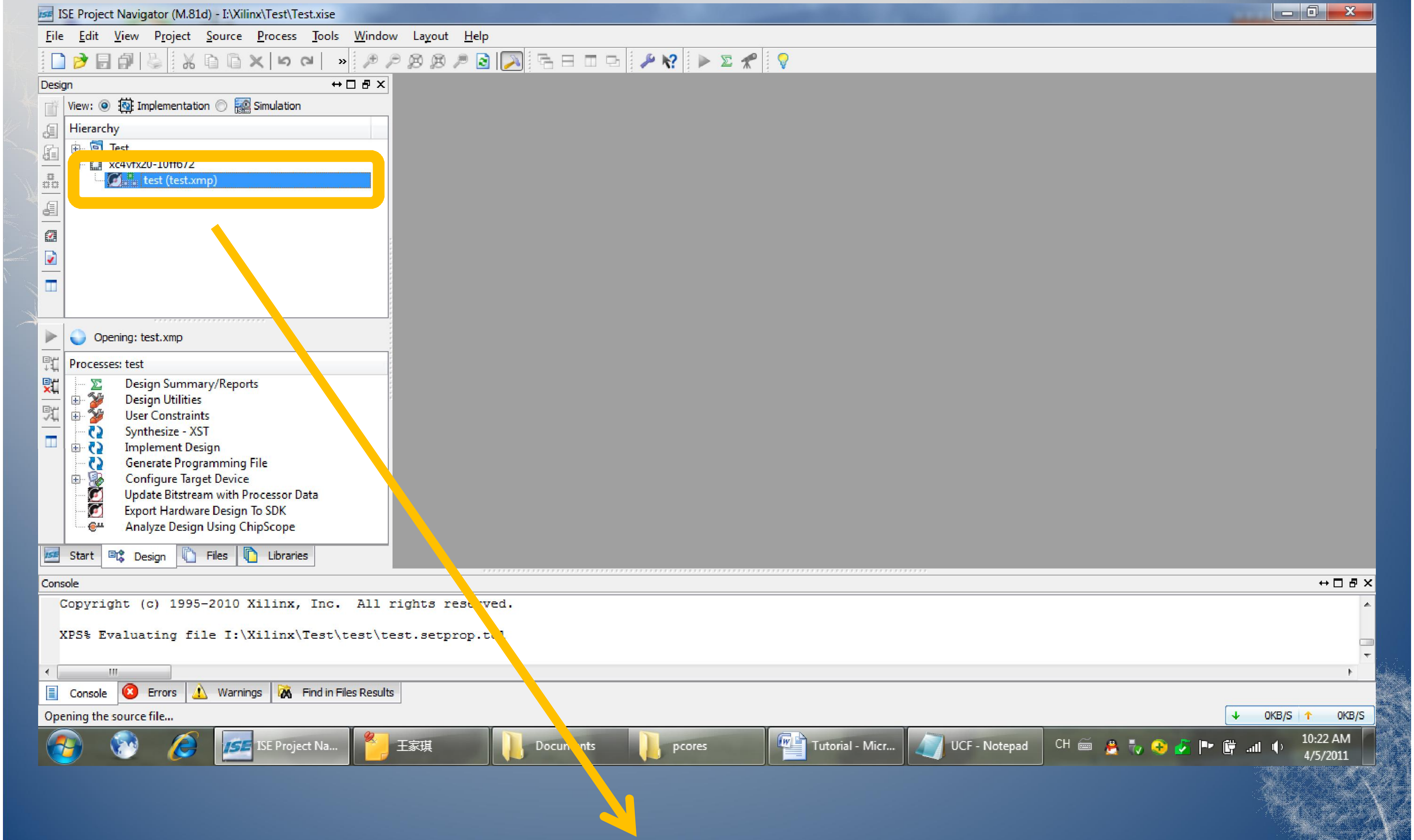
Find the motor wedge IP in the UserIPs folder


Computer ▸ TEMP (I:) ▸ Xilinx ▸ Test ▸ test ▸ pcores ▸
Search pcores
File Edit View Tools Help
Organize ▾ Open Include in library ▾ Share with ▾ Burn New folder
Favorites
Libraries
Homegroup
Computer
Windows XP (C:)
Windows 7 (D:)
Documents (E:)
Program (F:)
TEMP (I:)
Network

Name	Date modified	Type	Size
motor_wedge_v1_00_a	4/5/2011 10:20 AM	File folder	

motor_wedge_v1_00_a Date modified: 4/5/2011 10:20 AM
File folder

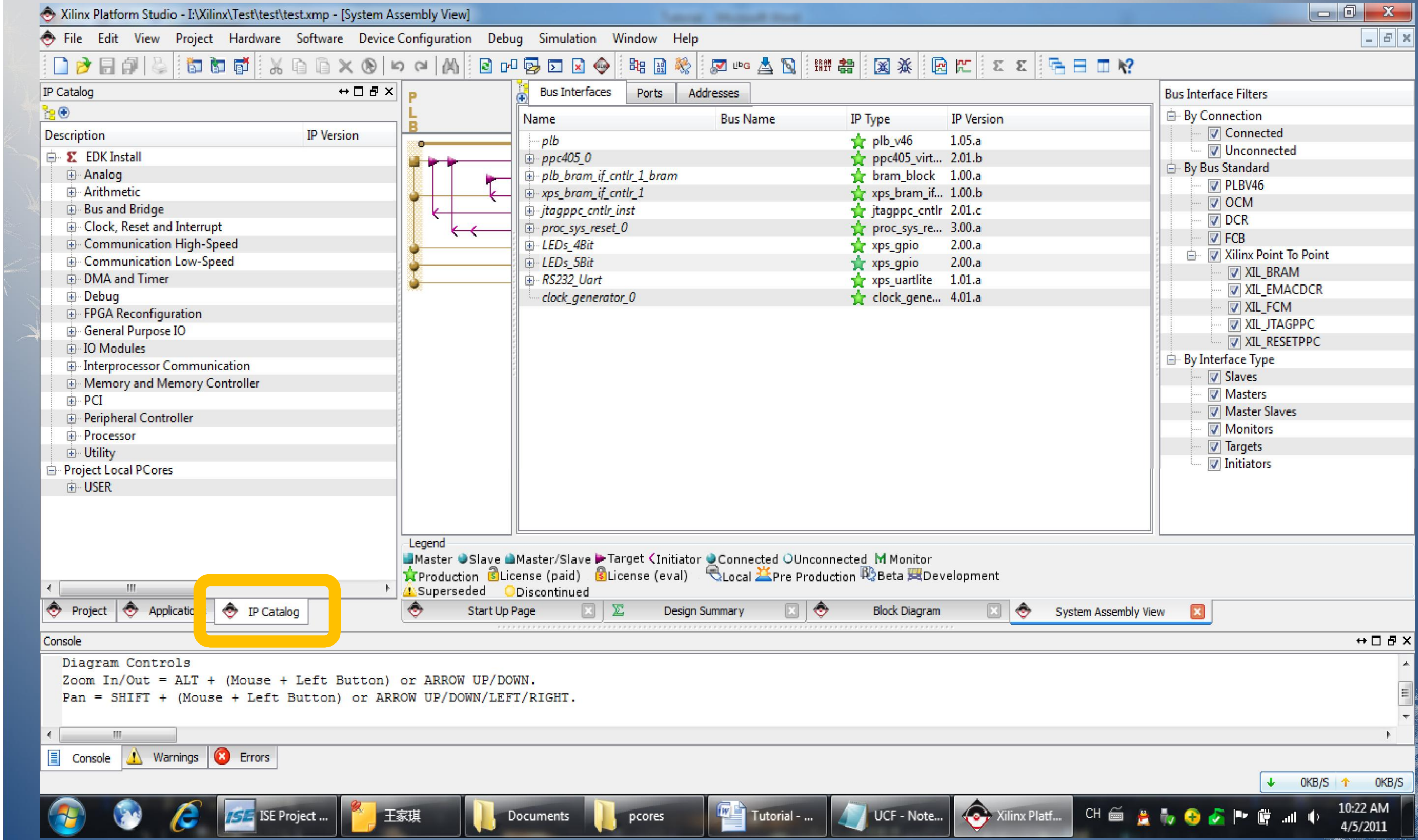
Copy the motor wedge IP to the “pcores” folder which is under “test”(embedded core we add in the ISE before) in the project folder ”Test”.



```
Copyright (c) 1995-2010 Xilinx, Inc.  All rights reserved.

XPS% Evaluating file I:\Xilinx\Test\test\test.setprop.tcl
```

Opening the source file...

Open XPS by double click on the test.xmp like before



IP Catalog

Description	IP Version
EDK Install	
Analog	
Arithmetic	
Bus and Bridge	
Clock, Reset and Interrupt	
Communication High-Speed	
Communication Low-Speed	
DMA and Timer	
Debug	
FPGA Reconfiguration	
General Purpose IO	
IO Modules	
Interprocessor Communication	
Memory and Memory Controller	
PCI	
Peripheral Controller	
Processor	
Utility	
Project Local PCores	
USER	

Name	Bus Name	IP Type	IP Version
plb		plb_v46	1.05.a
ppc405_0		ppc405_virt...	2.01.b
plb_bram_if_cntlr_1_bram		bram_block	1.00.a
xps_bram_if_cntlr_1		xps_bram_if...	1.00.b
jtagppc_cntlr_inst		jtagppc_cntlr	2.01.c
proc_sys_reset_0		proc_sys_re...	3.00.a
LEDs_4Bit		xps_gpio	2.00.a
LEDs_5Bit		xps_gpio	2.00.a
RS232_Uart		xps_uartlite	1.01.a
clock_generator_0		clock_gene...	4.01.a

Bus Interface Filters

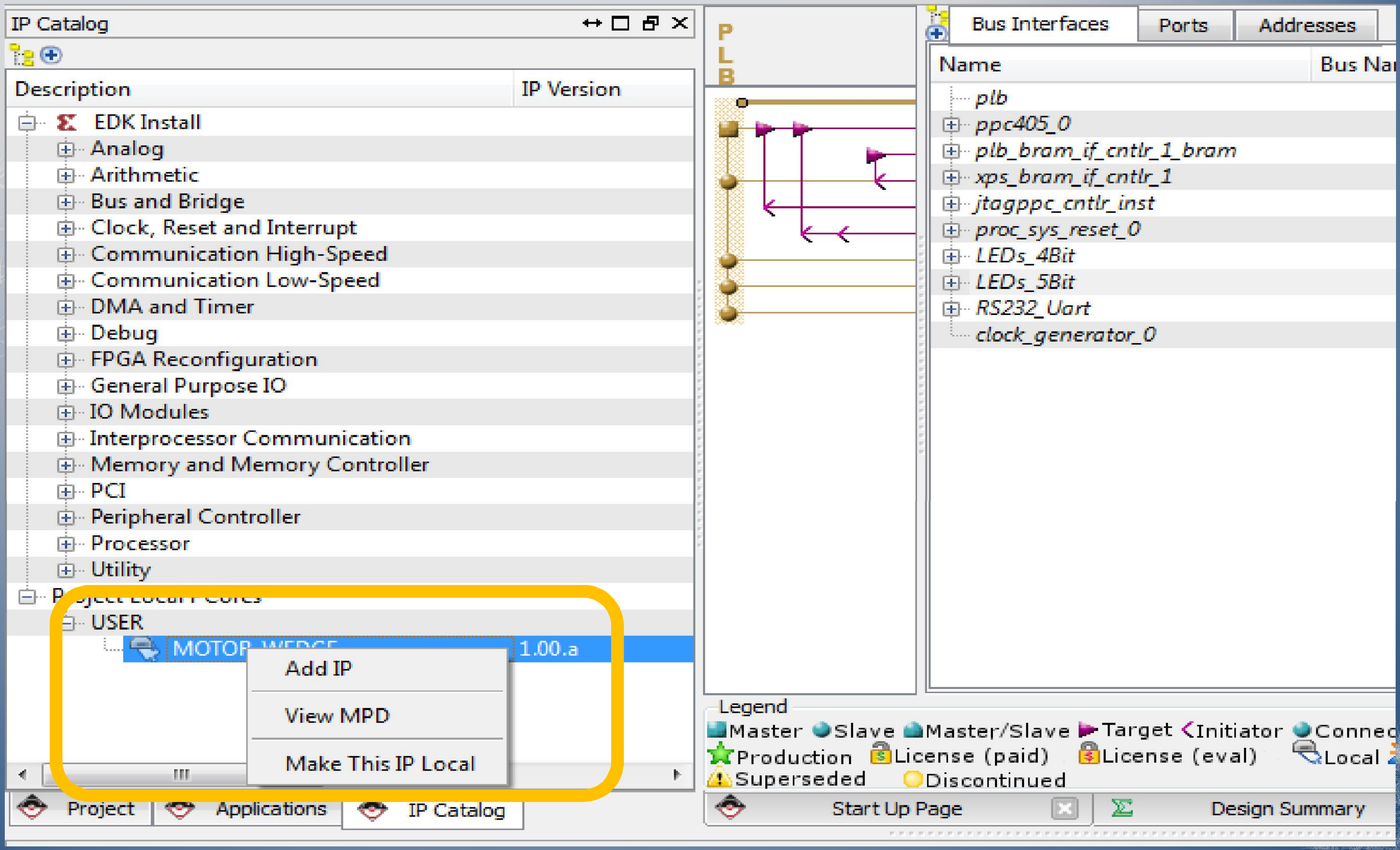
- By Connection
  - ☑ Connected
  - ☑ Unconnected
- By Bus Standard
  - ☑ PLBV46
  - ☑ OCM
  - ☑ DCR
  - ☑ FCB
  - ☑ Xilinx Point To Point
    - ☑ XIL_BRAM
    - ☑ XIL_EMACDCR
    - ☑ XIL_FCM
    - ☑ XIL_JTAGPPC
    - ☑ XIL_RESETPPC
- By Interface Type
  - ☑ Slaves
  - ☑ Masters
  - ☑ Master Slaves
  - ☑ Monitors
  - ☑ Targets
  - ☑ Initiators

Legend
Master Slave Master/Slave Target Initiator Connected Unconnected Monitor
Production License (paid) License (eval) Local Pre Production Beta Development
Superseded Discontinued

Console

```
Diagram Controls
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
```

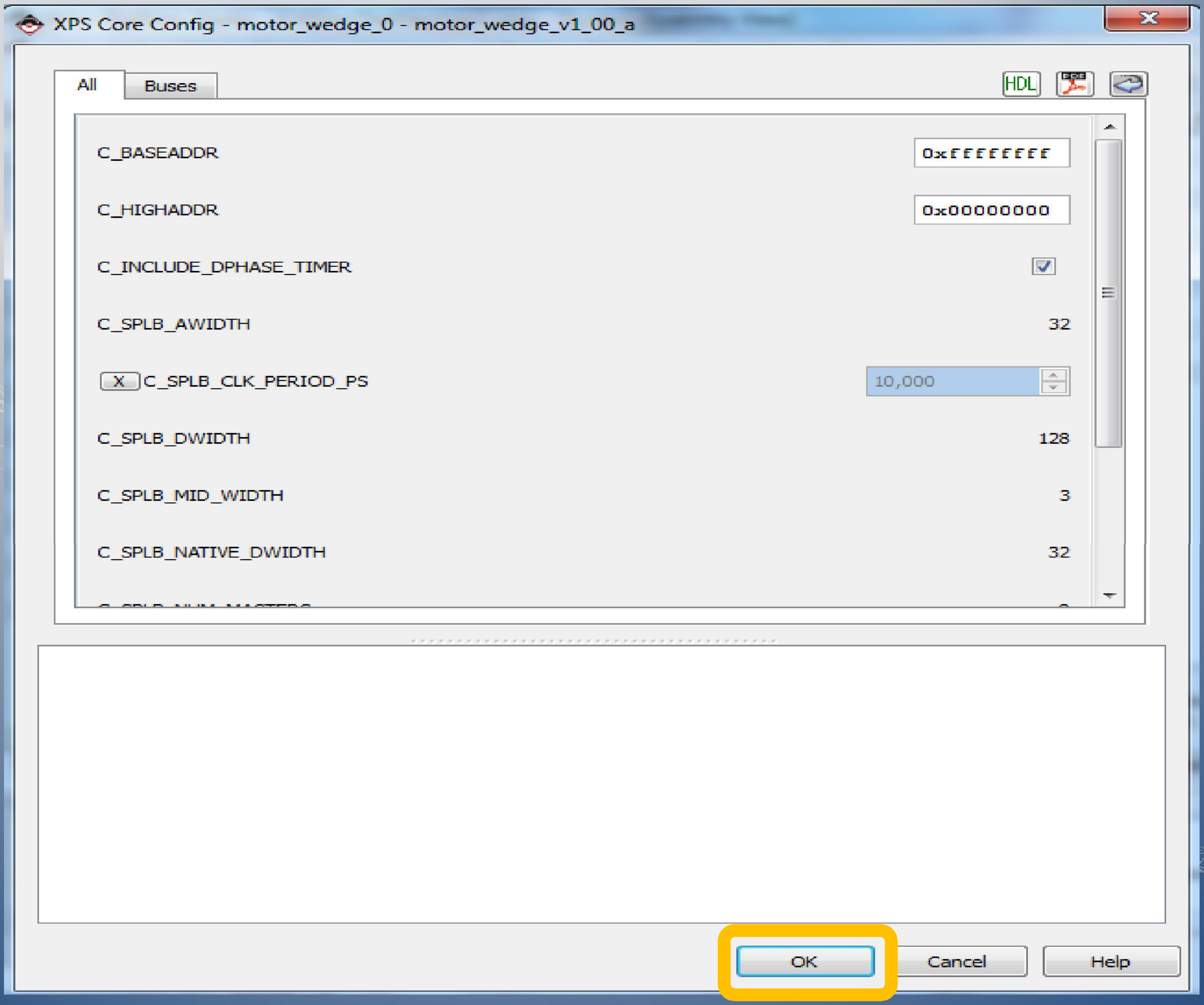
Now we come back to XPS



- EDK Install
  - Analog
  - Arithmetic
  - Bus and Bridge
  - Clock, Reset and Interrupt
  - Communication High-Speed
  - Communication Low-Speed
  - DMA and Timer
  - Debug
  - FPGA Reconfiguration
  - General Purpose IO
  - IO Modules
  - Interprocessor Communication
  - Memory and Memory Controller
  - PCI
  - Peripheral Controller
  - Processor
  - Utility
- Project Local Cores
  - USER
    - MOTOR_WEDGE 1.00.a

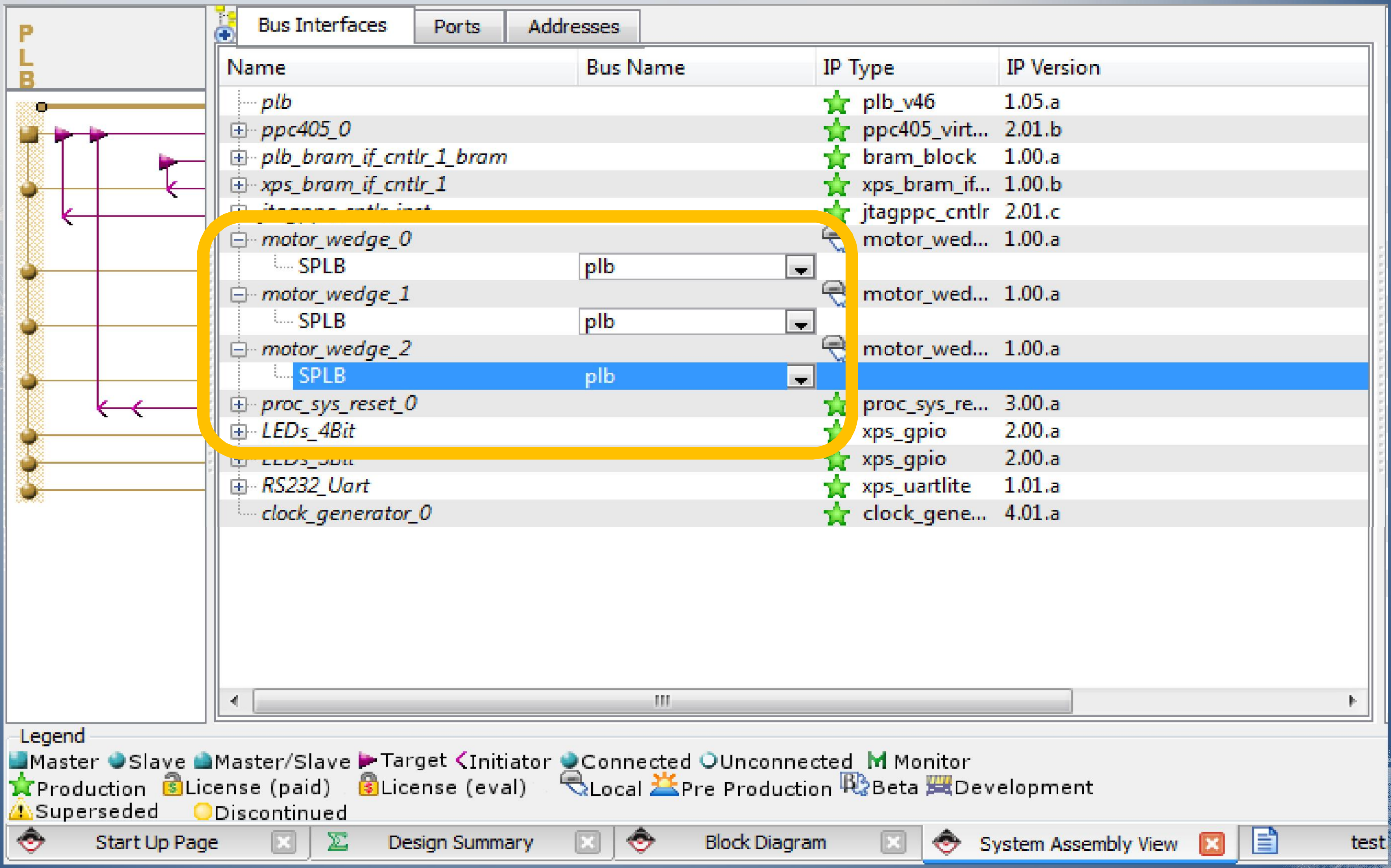
Name
plb
ppc405_0
plb_bram_if_cntlr_1_bram
xps_bram_if_cntlr_1
jtagppc_cntlr_inst
proc_sys_reset_0
LEDs_4Bit
LEDs_5Bit
RS232_Uart
clock_generator_0

This time we get USER IP in the list.
Add three MOTOR_WEDGE IP.



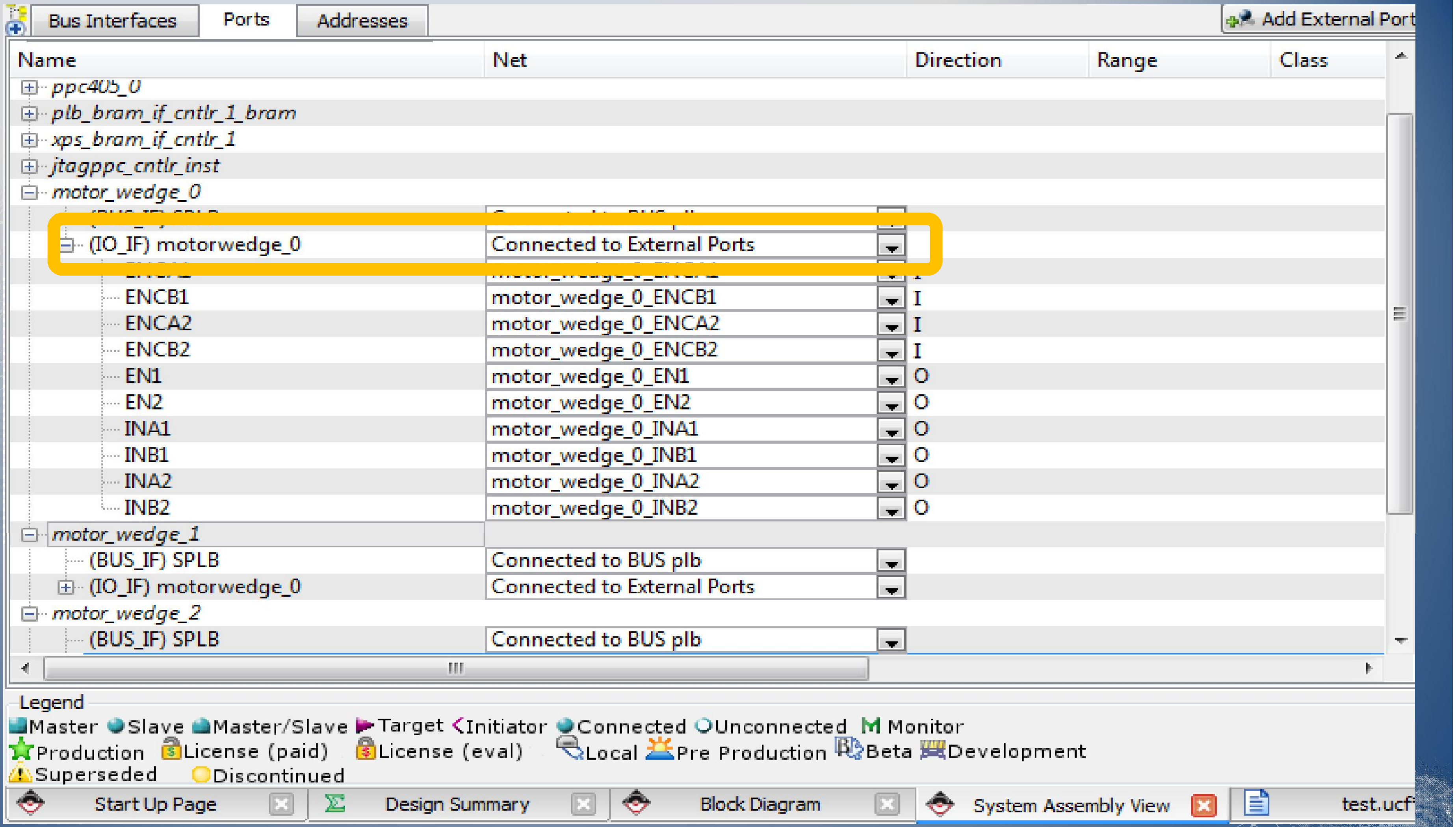
XPS Core Config - motor_wedge_0 - motor_wedge_v1_00_a

C_BASEADDR	0xffffffff
C_HIGHADDR	0x00000000
C_INCLUDE_DPHASE_TIMER	☑
C_SPLB_AWIDTH	32
X C_SPLB_CLK_PERIOD_PS	10,000
C_SPLB_DWIDTH	128
C_SPLB_MID_WIDTH	3
C_SPLB_NATIVE_DWIDTH	32



Name	Bus Name	IP Type	IP Version
plb		plb_v46	1.05.a
ppc405_0		ppc405_virt...	2.01.b
plb_bram_if_cntlr_1_bram		bram_block	1.00.a
xps_bram_if_cntlr_1		xps_bram_if...	1.00.b
jtagppc_cntlr_inst		jtagppc_cntlr	2.01.c
motor_wedge_0		motor_wed...	1.00.a
SPLB	plb		
motor_wedge_1		motor_wed...	1.00.a
SPLB	plb		
motor_wedge_2		motor_wed...	1.00.a
SPLB	plb		
proc_sys_reset_0		proc_sys_re...	3.00.a
LEDs_4Bit		xps_gpio	2.00.a
LEDs_8Bit		xps_gpio	2.00.a
RS232_Uart		xps_uartlite	1.01.a
clock_generator_0		clock_gene...	4.01.a

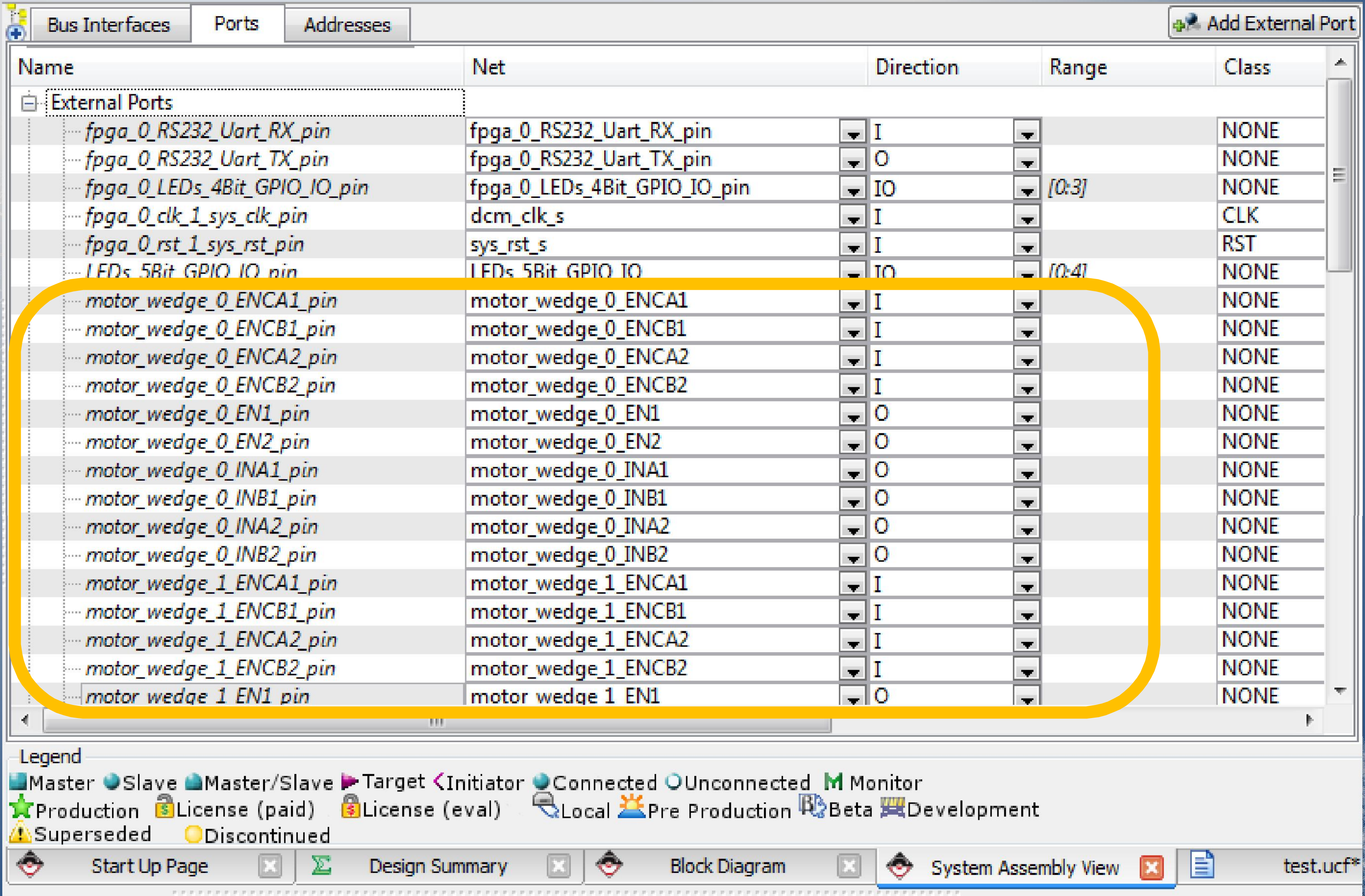
Connect these three MOTOR_WEDGE IP to plb bus.



Name	Net	Direction	Range	Class
⊞ *ppc405_0*				
⊞ *plb_bram_if_cntlr_1_bram*				
⊞ *xps_bram_if_cntlr_1*				
⊞ *jtagppc_cntlr_inst*				
⊟ *motor_wedge_0*				
(BUS_IF) SPLB	Connected to BUS plb			
⊟ (IO_IF) motorwedge_0	Connected to External Ports			
ENCA1	motor_wedge_0_ENCA1	I		
ENCB1	motor_wedge_0_ENCB1	I		
ENCA2	motor_wedge_0_ENCA2	I		
ENCB2	motor_wedge_0_ENCB2	I		
EN1	motor_wedge_0_EN1	O		
EN2	motor_wedge_0_EN2	O		
INA1	motor_wedge_0_INA1	O		
INB1	motor_wedge_0_INB1	O		
INA2	motor_wedge_0_INA2	O		
INB2	motor_wedge_0_INB2	O		
⊟ *motor_wedge_1*				
(BUS_IF) SPLB	Connected to BUS plb			
⊞ (IO_IF) motorwedge_0	Connected to External Ports			
⊟ *motor_wedge_2*				
(BUS_IF) SPLB	Connected to BUS plb			

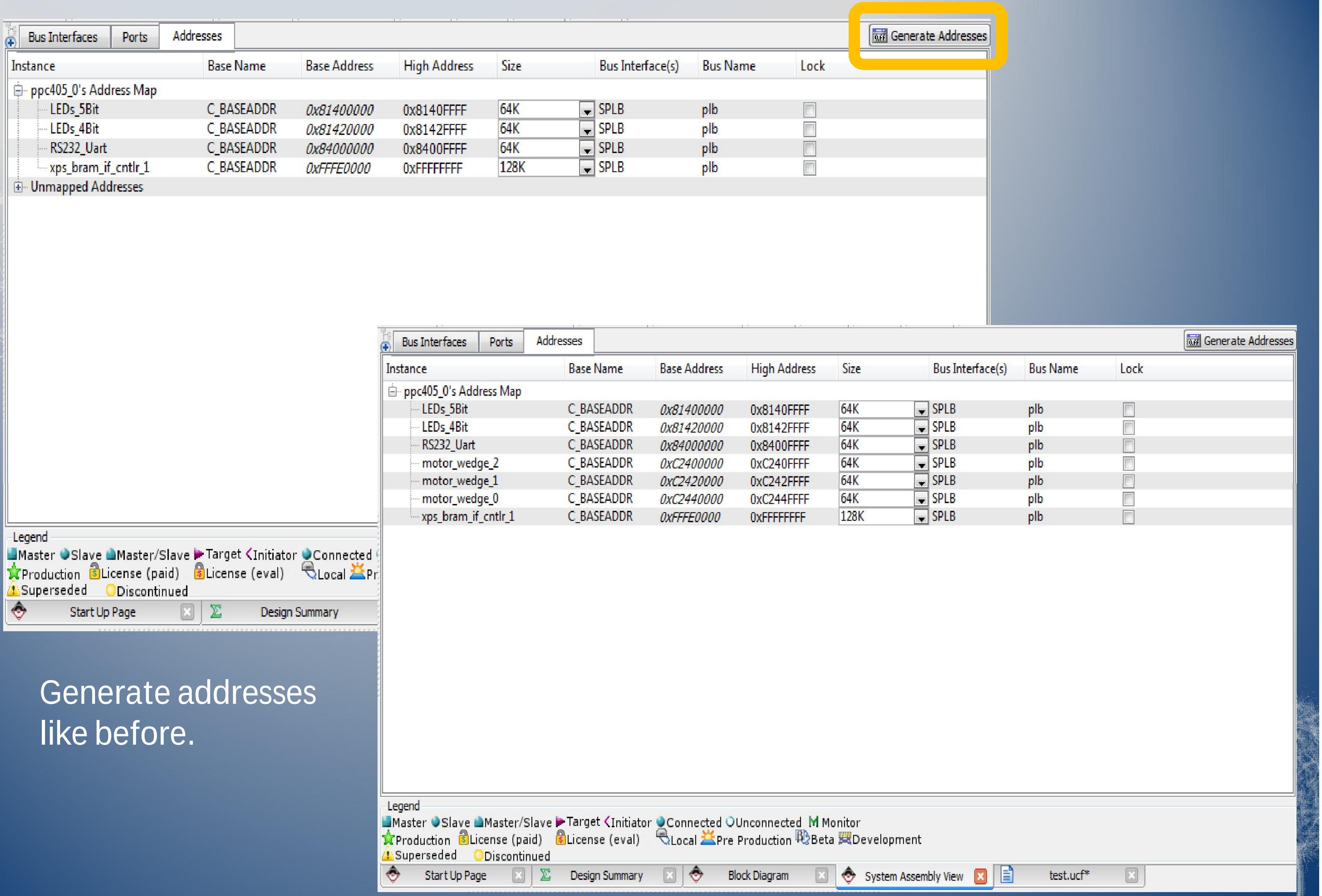
Legend
Master ● Slave Master/Slave Target Initiator ● Connected ○ Unconnected M Monitor
Production License (paid) License (eval) Local Pre Production Beta Development
Superseded ○ Discontinued

Connect their ports to external ports.



Name	Net	Direction	Range	Class
External Ports				
fpga_0_RS232_Uart_RX_pin	fpga_0_RS232_Uart_RX_pin	I		NONE
fpga_0_RS232_Uart_TX_pin	fpga_0_RS232_Uart_TX_pin	O		NONE
fpga_0_LEDs_4Bit_GPIO_IO_pin	fpga_0_LEDs_4Bit_GPIO_IO_pin	IO	[0:3]	NONE
fpga_0_clk_1_sys_clk_pin	dcm_clk_s	I		CLK
fpga_0_rst_1_sys_rst_pin	sys_rst_s	I		RST
LEDs_5Bit_GPIO_IO_pin	LEDs_5Bit_GPIO_IO	IO	[0:4]	NONE
motor_wedge_0_ENCA1_pin	motor_wedge_0_ENCA1	I		NONE
motor_wedge_0_ENCB1_pin	motor_wedge_0_ENCB1	I		NONE
motor_wedge_0_ENCA2_pin	motor_wedge_0_ENCA2	I		NONE
motor_wedge_0_ENCB2_pin	motor_wedge_0_ENCB2	I		NONE
motor_wedge_0_EN1_pin	motor_wedge_0_EN1	O		NONE
motor_wedge_0_EN2_pin	motor_wedge_0_EN2	O		NONE
motor_wedge_0_INA1_pin	motor_wedge_0_INA1	O		NONE
motor_wedge_0_INB1_pin	motor_wedge_0_INB1	O		NONE
motor_wedge_0_INA2_pin	motor_wedge_0_INA2	O		NONE
motor_wedge_0_INB2_pin	motor_wedge_0_INB2	O		NONE
motor_wedge_1_ENCA1_pin	motor_wedge_1_ENCA1	I		NONE
motor_wedge_1_ENCB1_pin	motor_wedge_1_ENCB1	I		NONE
motor_wedge_1_ENCA2_pin	motor_wedge_1_ENCA2	I		NONE
motor_wedge_1_ENCB2_pin	motor_wedge_1_ENCB2	I		NONE
motor_wedge_1_EN1_pin	motor_wedge_1_EN1	O		NONE

Check external ports.

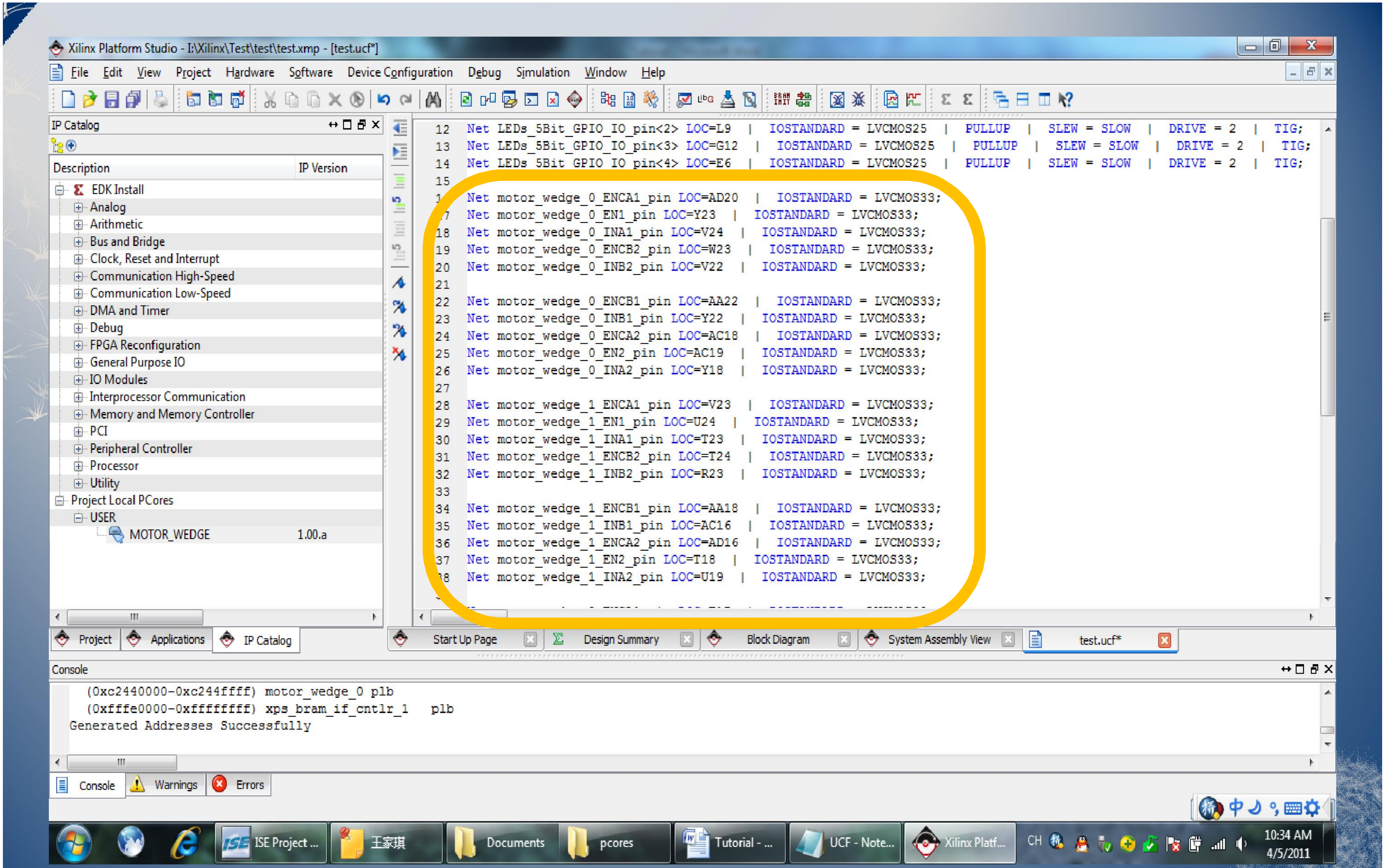

Bus Interfaces
Ports
Addresses
Generate Addresses
Legend
Master Slave Master/Slave Target Initiator Connected
Production License (paid) License (eval) Local Pr
Superseded Discontinued
Start Up Page
Design Summary

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
⊟ ppc405_0's Address Map							
LEDs_5Bit	C_BASEADDR	*0x81400000*	0x8140FFFF	64K	SPLB	plb	□
LEDs_4Bit	C_BASEADDR	*0x81420000*	0x8142FFFF	64K	SPLB	plb	□
RS232_Uart	C_BASEADDR	*0x84000000*	0x8400FFFF	64K	SPLB	plb	□
xps_bram_if_cntlr_1	C_BASEADDR	*0xFFFE0000*	0xFFFFFFFF	128K	SPLB	plb	□
⊞ Unmapped Addresses							

Bus Interfaces
Ports
Addresses
Generate Addresses
Legend
Master Slave Master/Slave Target Initiator Connected Unconnected Monitor
Production License (paid) License (eval) Local Pre Production Beta Development
Superseded Discontinued
Start Up Page
Design Summary
Block Diagram
System Assembly View
test.ucf*

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
⊟ ppc405_0's Address Map							
LEDs_5Bit	C_BASEADDR	*0x81400000*	0x8140FFFF	64K	SPLB	plb	□
LEDs_4Bit	C_BASEADDR	*0x81420000*	0x8142FFFF	64K	SPLB	plb	□
RS232_Uart	C_BASEADDR	*0x84000000*	0x8400FFFF	64K	SPLB	plb	□
motor_wedge_2	C_BASEADDR	*0xC2400000*	0xC240FFFF	64K	SPLB	plb	□
motor_wedge_1	C_BASEADDR	*0xC2420000*	0xC242FFFF	64K	SPLB	plb	□
motor_wedge_0	C_BASEADDR	*0xC2440000*	0xC244FFFF	64K	SPLB	plb	□
xps_bram_if_cntlr_1	C_BASEADDR	*0xFFFE0000*	0xFFFFFFFF	128K	SPLB	plb	□

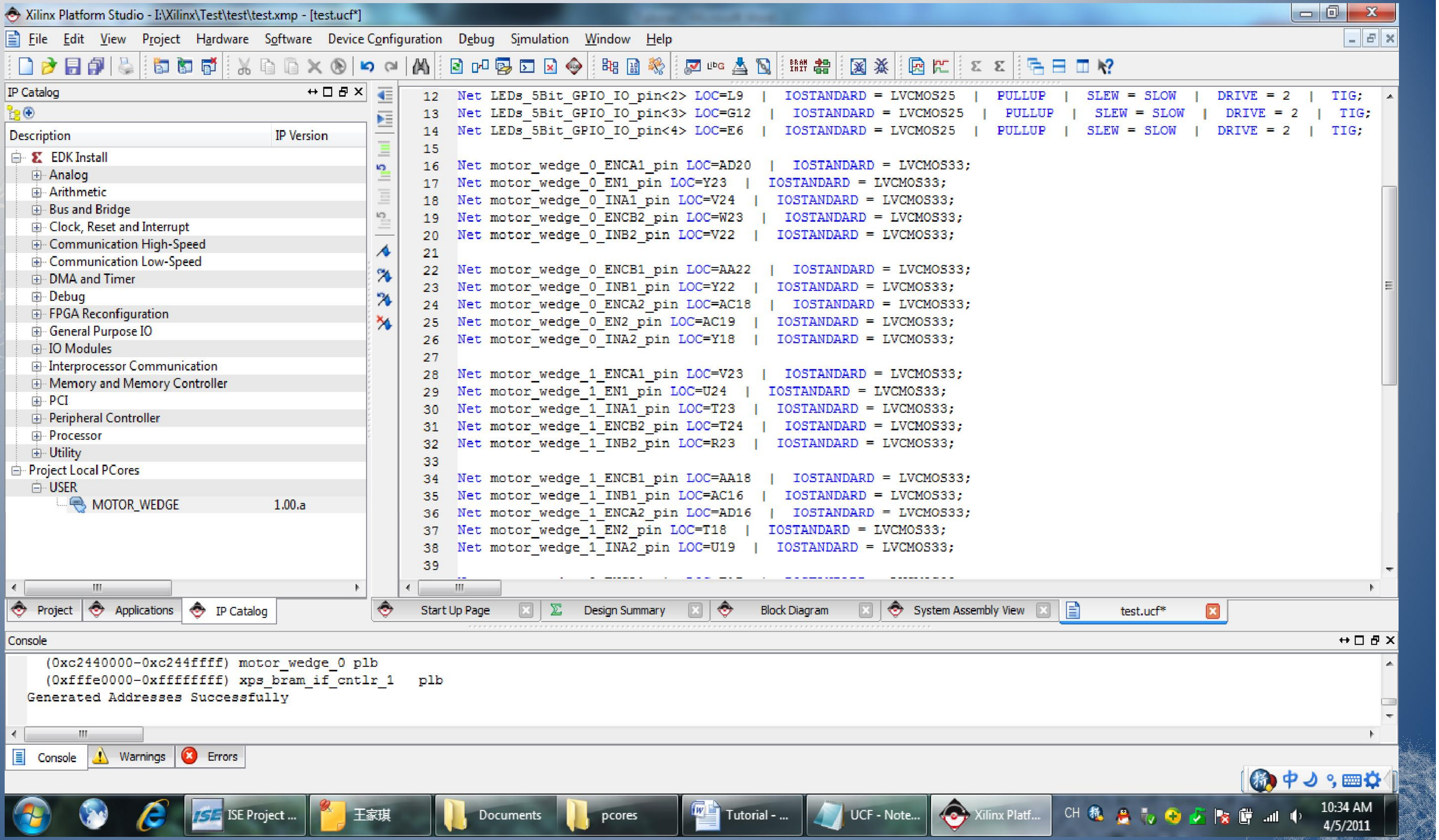
Generate addresses like before.



```
Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;

Net motor_wedge_0_ENCA1_pin LOC=AD20  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN1_pin LOC=Y23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA1_pin LOC=V24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCB2_pin LOC=W23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB2_pin LOC=V22  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_0_ENCB1_pin LOC=AA22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB1_pin LOC=Y22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCA2_pin LOC=AC18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN2_pin LOC=AC19  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA2_pin LOC=Y18  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_1_ENCA1_pin LOC=V23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_EN1_pin LOC=U24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INA1_pin LOC=T23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_ENCB2_pin LOC=T24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INB2_pin LOC=R23  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_1_ENCB1_pin LOC=AA18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INB1_pin LOC=AC16  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_ENCA2_pin LOC=AD16  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_EN2_pin LOC=T18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INA2_pin LOC=U19  |  IOSTANDARD = LVCMOS33;
```

```
  (0xc2440000-0xc244ffff) motor_wedge_0 plb
  (0xfffe0000-0xffffffff) xps_bram_if_cntlr_1   plb
Generated Addresses Successfully
```

Copy these from UCF text document into the UCF file in XPS like before.



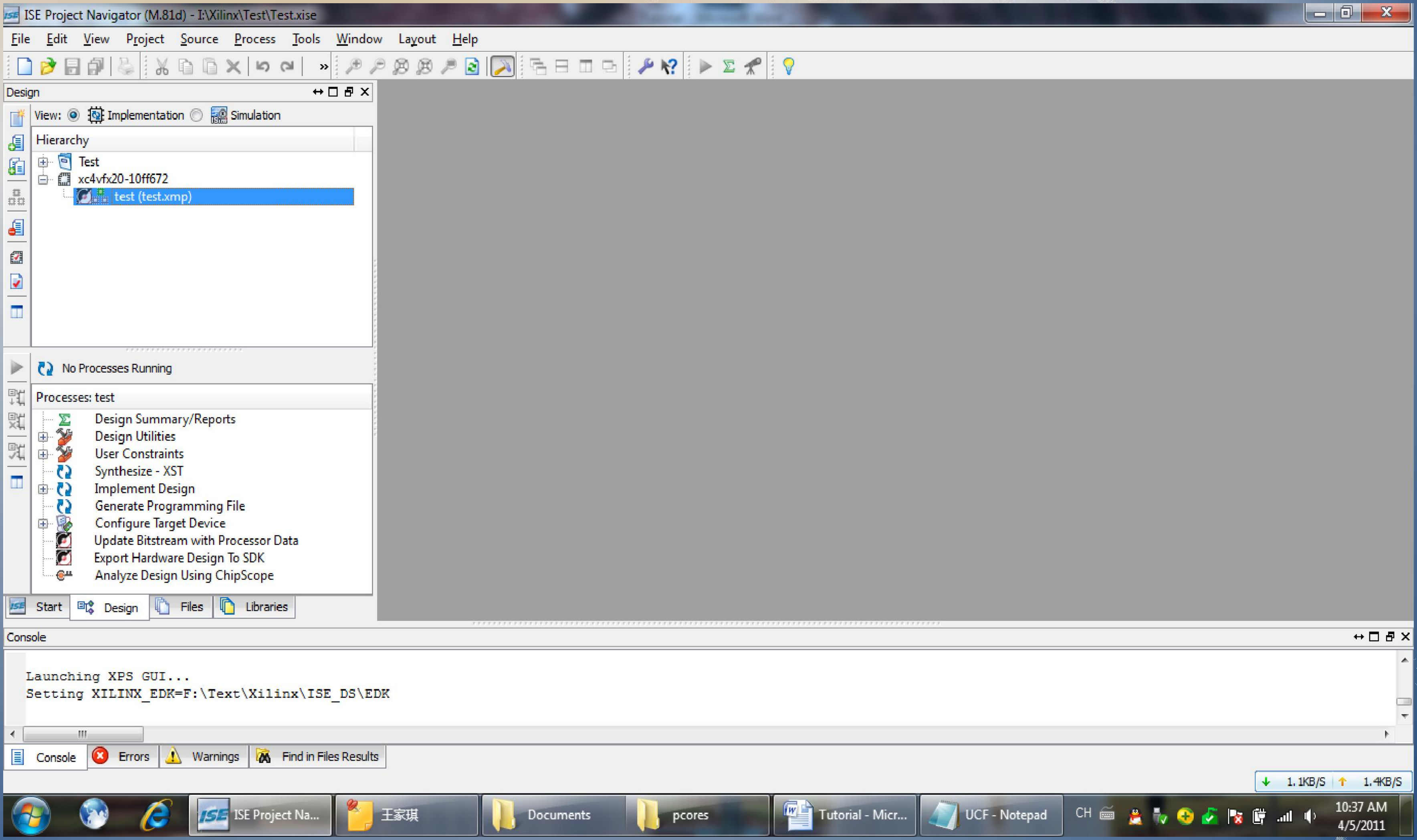
```
Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;

Net motor_wedge_0_ENCA1_pin LOC=AD20  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN1_pin LOC=Y23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA1_pin LOC=V24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCB2_pin LOC=W23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB2_pin LOC=V22  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_0_ENCB1_pin LOC=AA22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB1_pin LOC=Y22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCA2_pin LOC=AC18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN2_pin LOC=AC19  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA2_pin LOC=Y18  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_1_ENCA1_pin LOC=V23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_EN1_pin LOC=U24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INA1_pin LOC=T23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_ENCB2_pin LOC=T24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INB2_pin LOC=R23  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_1_ENCB1_pin LOC=AA18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INB1_pin LOC=AC16  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_ENCA2_pin LOC=AD16  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_EN2_pin LOC=T18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_1_INA2_pin LOC=U19  |  IOSTANDARD = LVCMOS33;
```

```
   (0xc2440000-0xc244ffff) motor_wedge_0 plb
   (0xfffe0000-0xffffffff) xps_bram_if_cntlr_1   plb
Generated Addresses Successfully
```

Adding IPs is completed. Exit XPS and go back to ISE.

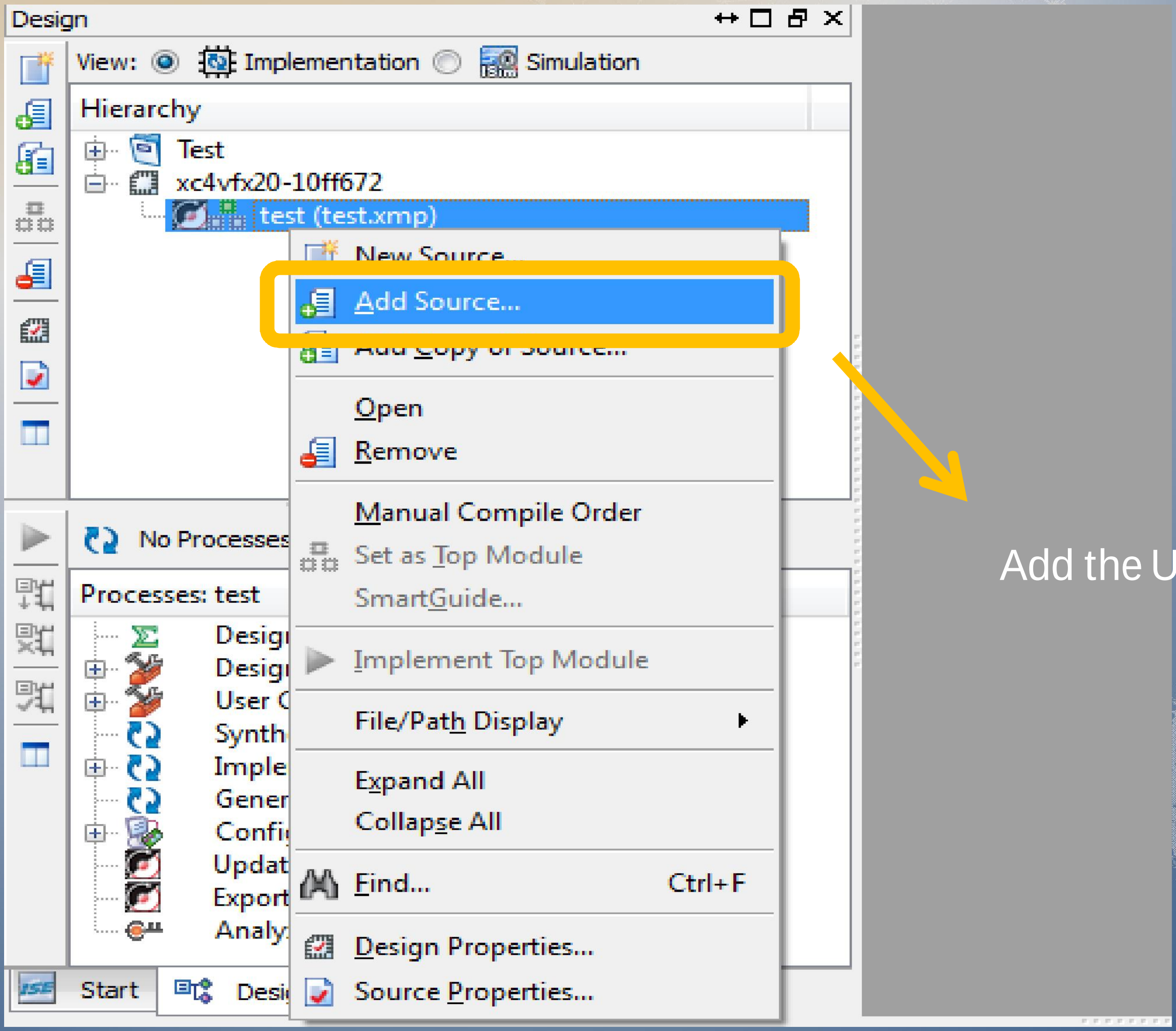
Part IV:
Create a Software Project in SDK

This part will show you how to actually put some codes in this project and run it in FPGA.

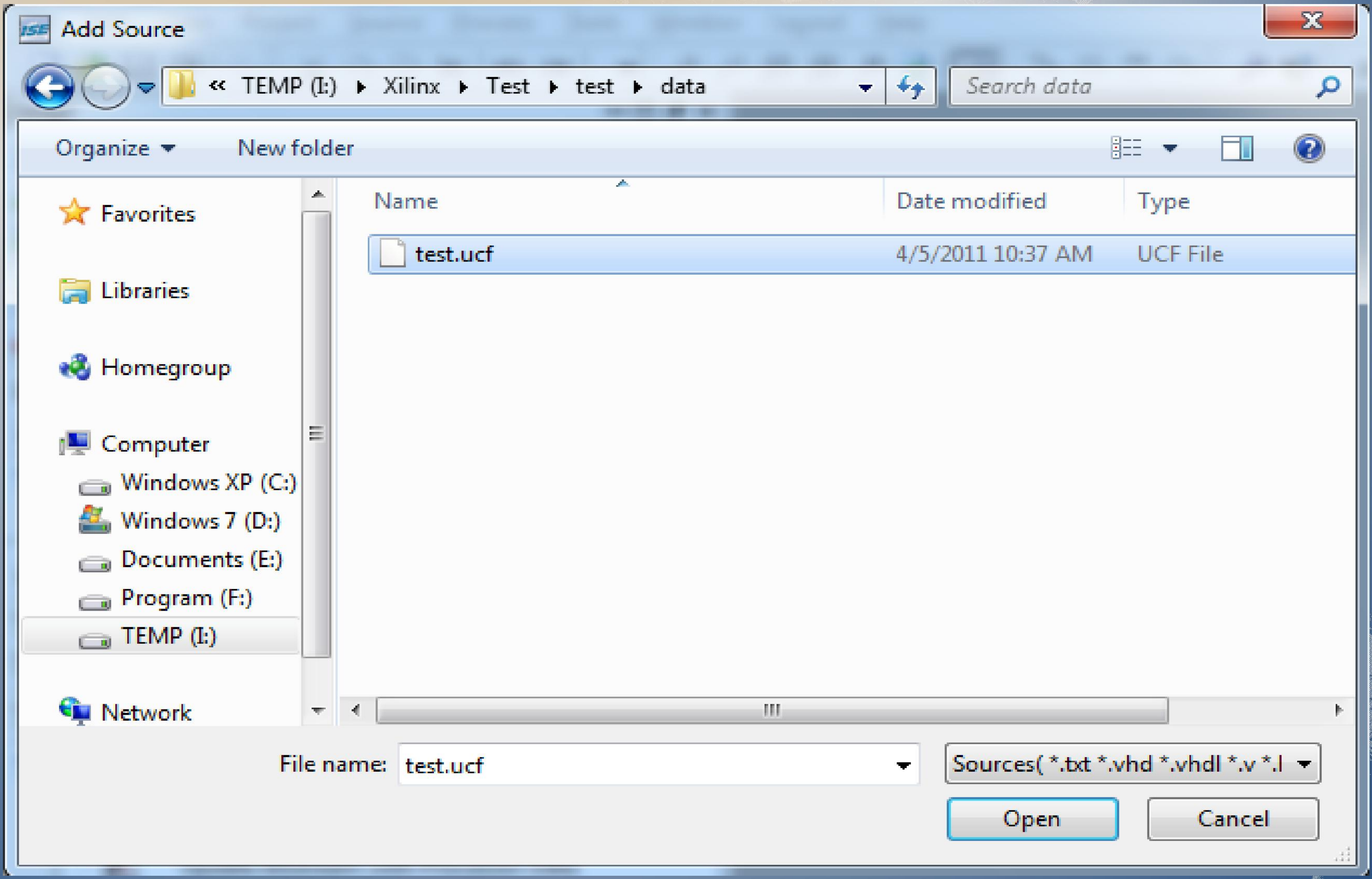


```
Launching XPS GUI...
Setting XILINX_EDK=F:\Text\Xilinx\ISE_DS\EDK
```

Before opening SDK, we need to export hardware design to it in ISE.



Add the UCF file.

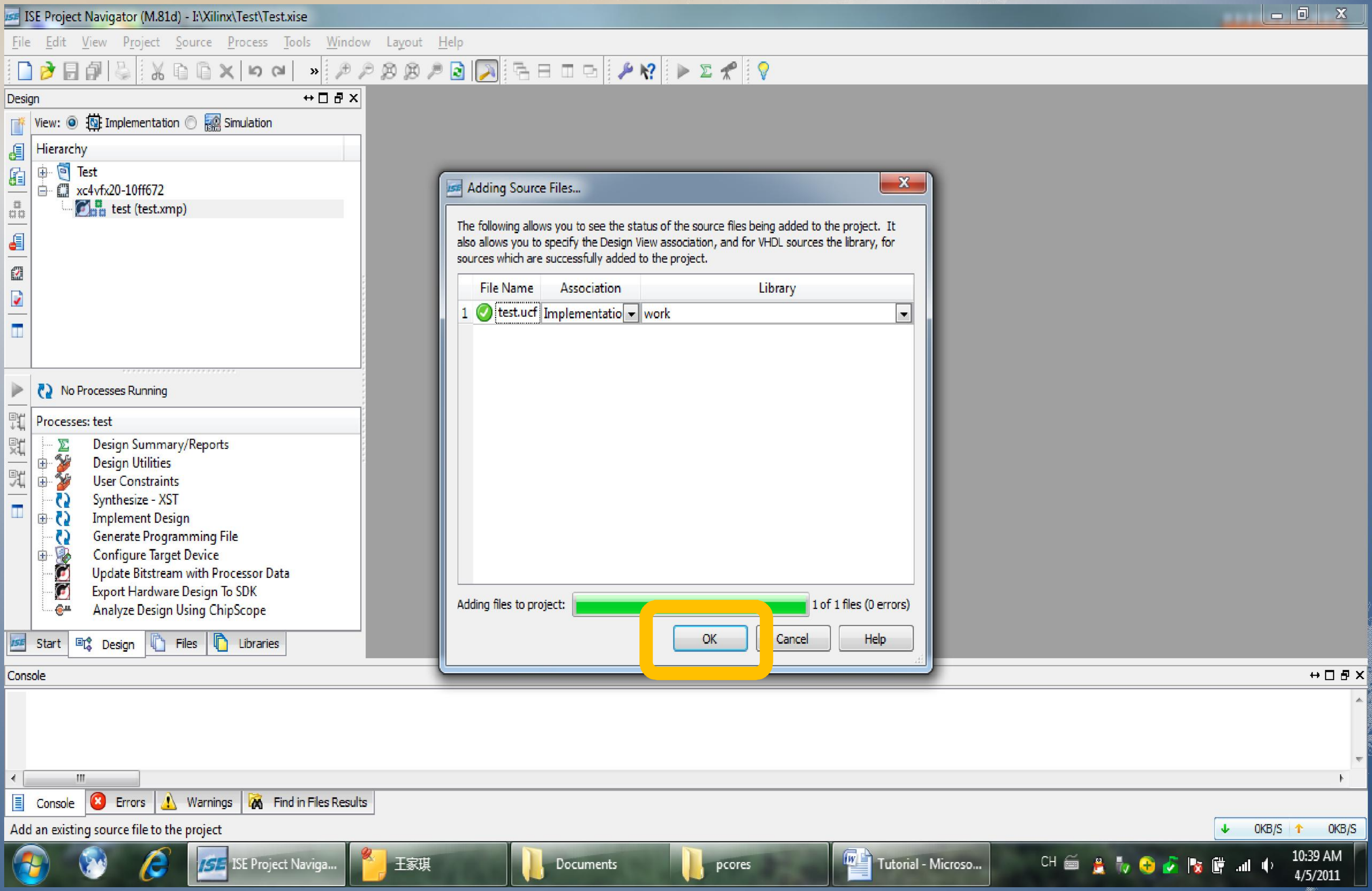


Name	Date modified	Type
test.ucf	4/5/2011 10:37 AM	UCF File

File name: test.ucf

Sources(*.txt *.vhd *.vhdl *.v *.l

The UCF file is under the “data” folder in the “test”(embedded core) of the project folder “Test”.

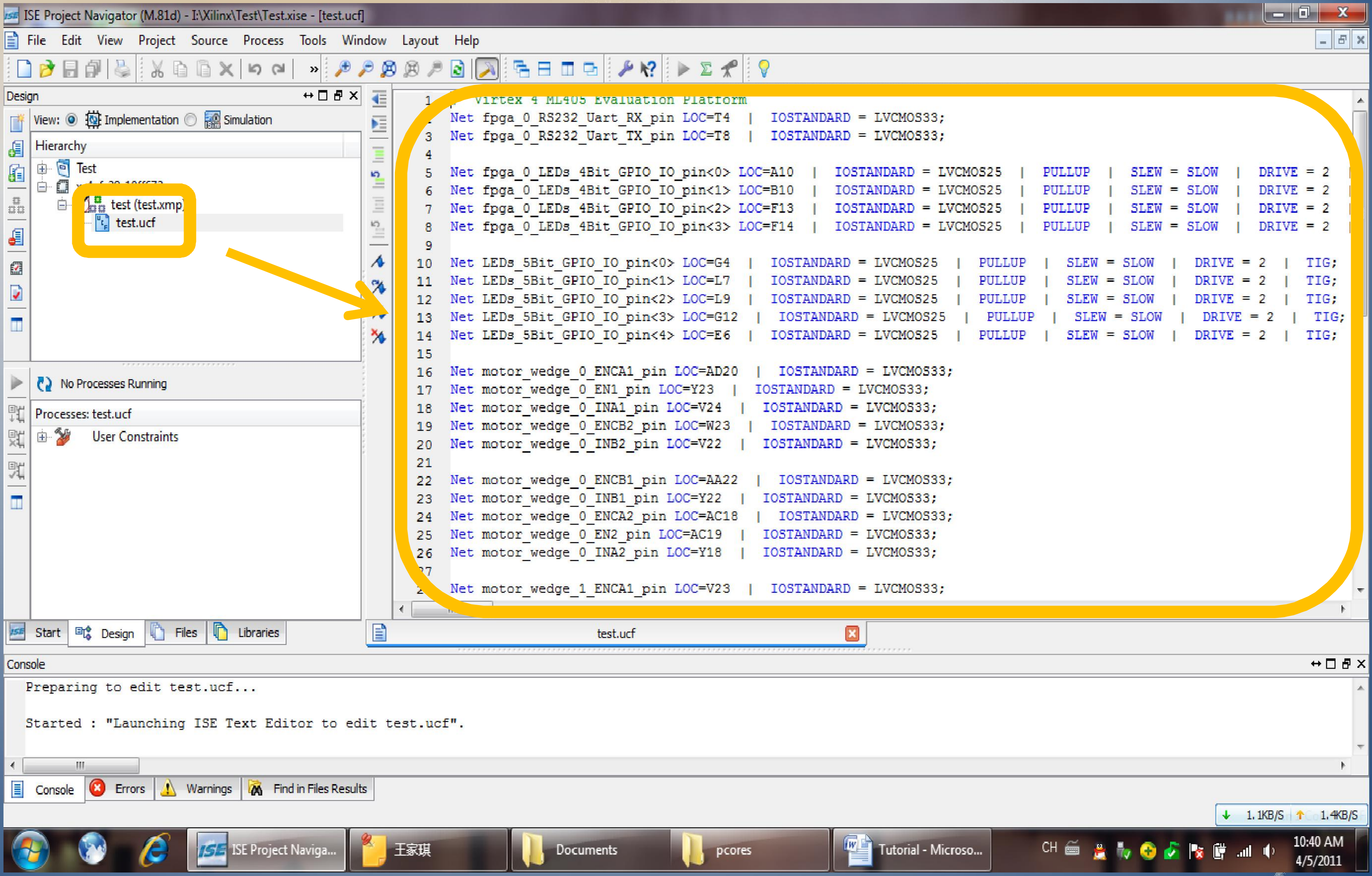


Adding Source Files...

The following allows you to see the status of the source files being added to the project. It also allows you to specify the Design View association, and for VHDL sources the library, for sources which are successfully added to the project.

	File Name	Association	Library
1	✓ test.ucf	Implementatio	work

Adding files to project: 1 of 1 files (0 errors)

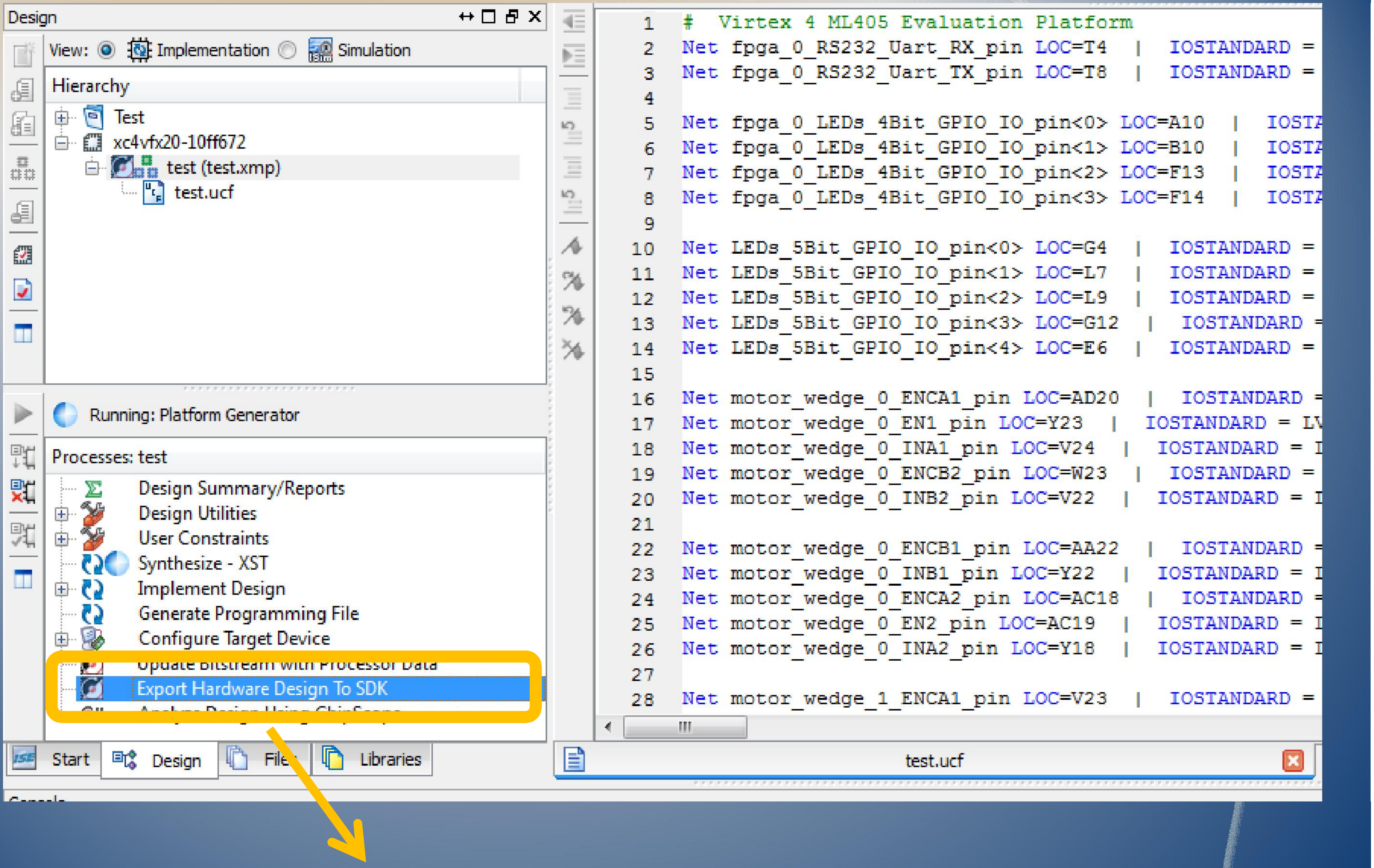


ISE Project Navigator (M.81d) - I:\Xilinx\Test\Test.xise - [test.ucf]
File Edit View Project Source Process Tools Window Layout Help
Design
View: ● Implementation ○ Simulation
Hierarchy
Test
test (test.xmp)
test.ucf
No Processes Running
Processes: test.ucf
User Constraints
Start Design Files Libraries
test.ucf
Console
Console Errors Warnings Find in Files Results
1.1KB/S 1.4KB/S
ISE Project Naviga...
王家琪
Documents
pcores
Tutorial - Microso...
CH
10:40 AM
4/5/2011

```
  Virtex 4 ML405 Evaluation Platform
Net fpga_0_RS232_Uart_RX_pin LOC=T4  |  IOSTANDARD = LVCMOS33;
Net fpga_0_RS232_Uart_TX_pin LOC=T8  |  IOSTANDARD = LVCMOS33;

Net fpga_0_LEDs_4Bit_GPIO_IO_pin<0> LOC=A10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<1> LOC=B10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<2> LOC=F13  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<3> LOC=F14  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |

Net LEDs_5Bit_GPIO_IO_pin<0> LOC=G4  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<1> LOC=L7  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;

Net motor_wedge_0_ENCA1_pin LOC=AD20  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN1_pin LOC=Y23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA1_pin LOC=V24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCB2_pin LOC=W23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB2_pin LOC=V22  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_0_ENCB1_pin LOC=AA22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB1_pin LOC=Y22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCA2_pin LOC=AC18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN2_pin LOC=AC19  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA2_pin LOC=Y18  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_1_ENCA1_pin LOC=V23  |  IOSTANDARD = LVCMOS33;
```

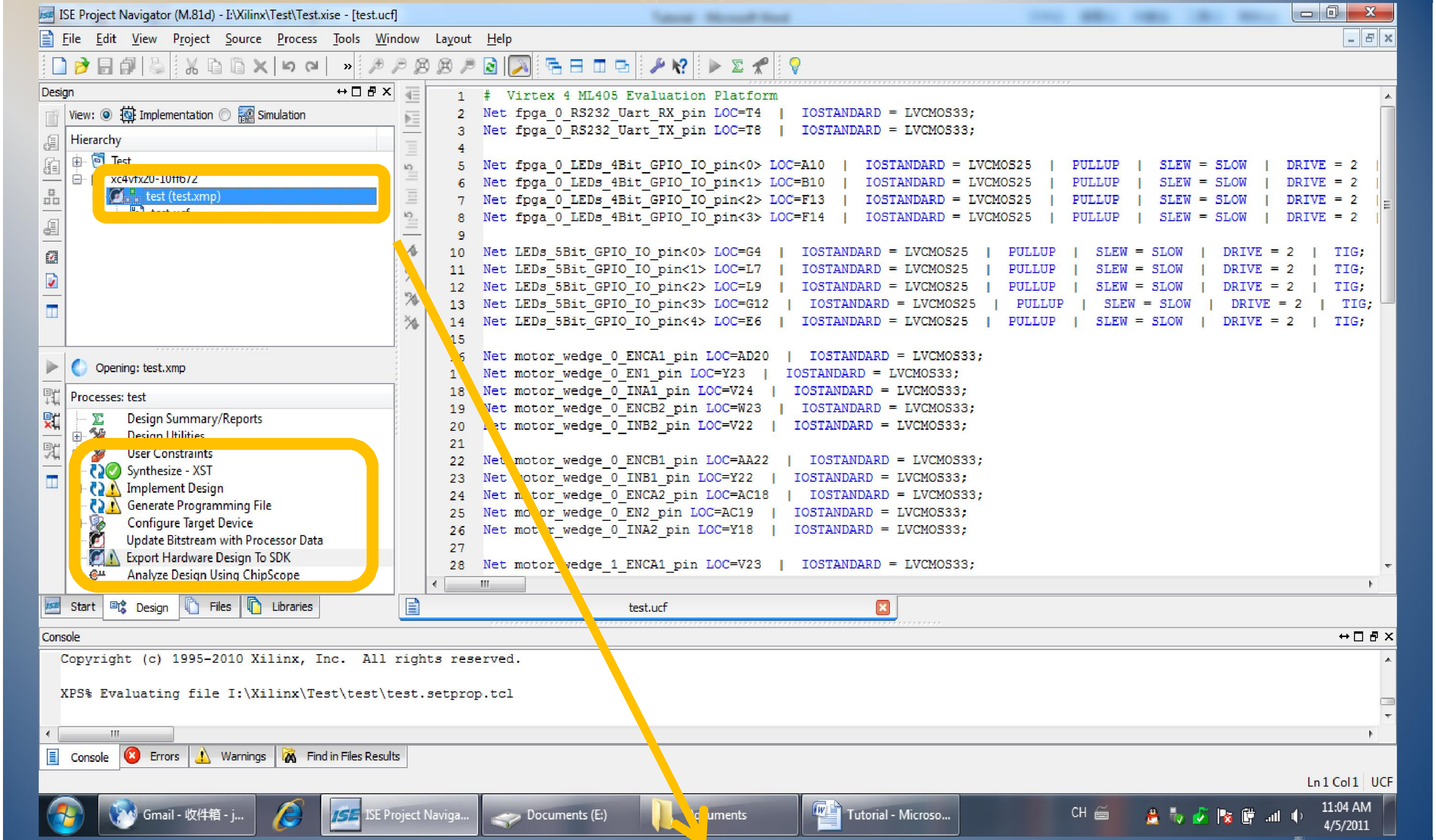
```
Preparing to edit test.ucf...

Started : "Launching ISE Text Editor to edit test.ucf".
```

Check the UCF file.



```
#  Virtex 4 ML405 Evaluation Platform
Net fpga_0_RS232_Uart_RX_pin LOC=T4  |  IOSTANDARD =
Net fpga_0_RS232_Uart_TX_pin LOC=T8  |  IOSTANDARD =

Net fpga_0_LEDs_4Bit_GPIO_IO_pin<0> LOC=A10  |  IOSTA
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<1> LOC=B10  |  IOSTA
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<2> LOC=F13  |  IOSTA
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<3> LOC=F14  |  IOSTA

Net LEDs_5Bit_GPIO_IO_pin<0> LOC=G4  |  IOSTANDARD =
Net LEDs_5Bit_GPIO_IO_pin<1> LOC=L7  |  IOSTANDARD =
Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9  |  IOSTANDARD =
Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12  |  IOSTANDARD =
Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6  |  IOSTANDARD =

Net motor_wedge_0_ENCA1_pin LOC=AD20  |  IOSTANDARD =
Net motor_wedge_0_EN1_pin LOC=Y23  |  IOSTANDARD = LV
Net motor_wedge_0_INA1_pin LOC=V24  |  IOSTANDARD = I
Net motor_wedge_0_ENCB2_pin LOC=W23  |  IOSTANDARD =
Net motor_wedge_0_INB2_pin LOC=V22  |  IOSTANDARD = I

Net motor_wedge_0_ENCB1_pin LOC=AA22  |  IOSTANDARD =
Net motor_wedge_0_INB1_pin LOC=Y22  |  IOSTANDARD = I
Net motor_wedge_0_ENCA2_pin LOC=AC18  |  IOSTANDARD =
Net motor_wedge_0_EN2_pin LOC=AC19  |  IOSTANDARD = I
Net motor_wedge_0_INA2_pin LOC=Y18  |  IOSTANDARD = I

Net motor_wedge_1_ENCA1_pin LOC=V23  |  IOSTANDARD =
```

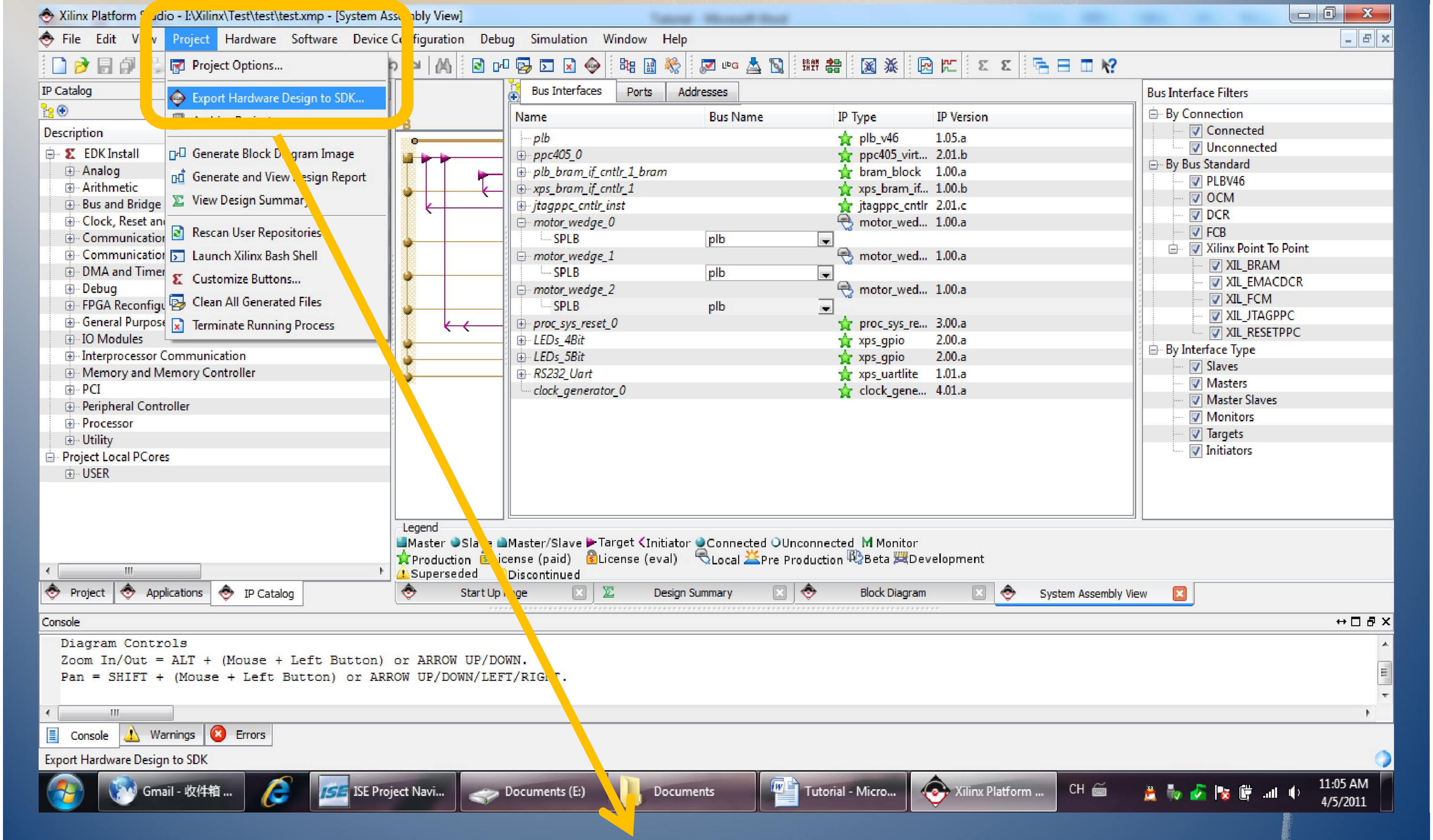
Double click on it to export hardware design to SDK. This might take several minuets.



```
#  Virtex 4 ML405 Evaluation Platform
Net fpga_0_RS232_Uart_RX_pin LOC=T4  |  IOSTANDARD = LVCMOS33;
Net fpga_0_RS232_Uart_TX_pin LOC=T8  |  IOSTANDARD = LVCMOS33;

Net fpga_0_LEDs_4Bit_GPIO_IO_pin<0> LOC=A10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<1> LOC=B10  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<2> LOC=F13  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |
Net fpga_0_LEDs_4Bit_GPIO_IO_pin<3> LOC=F14  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |

Net LEDs_5Bit_GPIO_IO_pin<0> LOC=G4  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<1> LOC=L7  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;
Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6  |  IOSTANDARD = LVCMOS25  |  PULLUP  |  SLEW = SLOW  |  DRIVE = 2  |  TIG;

Net motor_wedge_0_ENCA1_pin LOC=AD20  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN1_pin LOC=Y23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA1_pin LOC=V24  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCB2_pin LOC=W23  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB2_pin LOC=V22  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_0_ENCB1_pin LOC=AA22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INB1_pin LOC=Y22  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_ENCA2_pin LOC=AC18  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_EN2_pin LOC=AC19  |  IOSTANDARD = LVCMOS33;
Net motor_wedge_0_INA2_pin LOC=Y18  |  IOSTANDARD = LVCMOS33;

Net motor_wedge_1_ENCA1_pin LOC=V23  |  IOSTANDARD = LVCMOS33;
```

```
Copyright (c) 1995-2010 Xilinx, Inc.  All rights reserved.

XPS% Evaluating file I:\Xilinx\Test\test\test.setprop.tcl
```

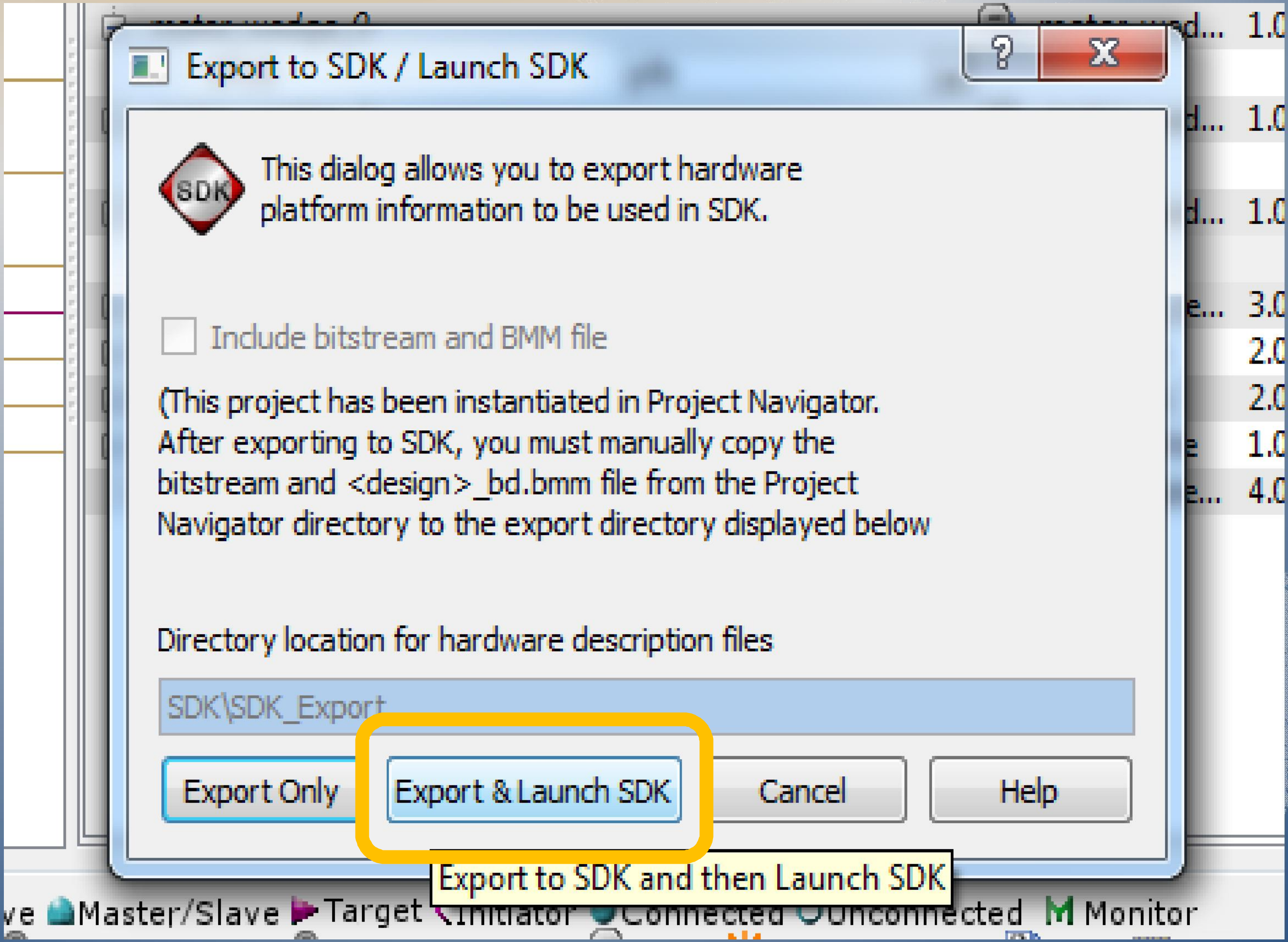
When export process is done, double click on the test.xmp to open XPS .



Name	Bus Name	IP Type	IP Version
plb		plb_v46	1.05.a
ppc405_0		ppc405_virt...	2.01.b
plb_bram_if_cntlr_1_bram		bram_block	1.00.a
xps_bram_if_cntlr_1		xps_bram_if...	1.00.b
jtagppc_cntlr_inst		jtagppc_cntlr	2.01.c
motor_wedge_0		motor_wed...	1.00.a
SPLB	plb		
motor_wedge_1		motor_wed...	1.00.a
SPLB	plb		
motor_wedge_2		motor_wed...	1.00.a
SPLB	plb		
proc_sys_reset_0		proc_sys_re...	3.00.a
LEDs_4Bit		xps_gpio	2.00.a
LEDs_5Bit		xps_gpio	2.00.a
RS232_Uart		xps_uartlite	1.01.a
clock_generator_0		clock_gene...	4.01.a

```
Diagram Controls
Zoom In/Out = ALT + (Mouse + Left Button) or ARROW UP/DOWN.
Pan = SHIFT + (Mouse + Left Button) or ARROW UP/DOWN/LEFT/RIGHT.
```

Open SDK from here.



Export to SDK / Launch SDK

This dialog allows you to export hardware platform information to be used in SDK.

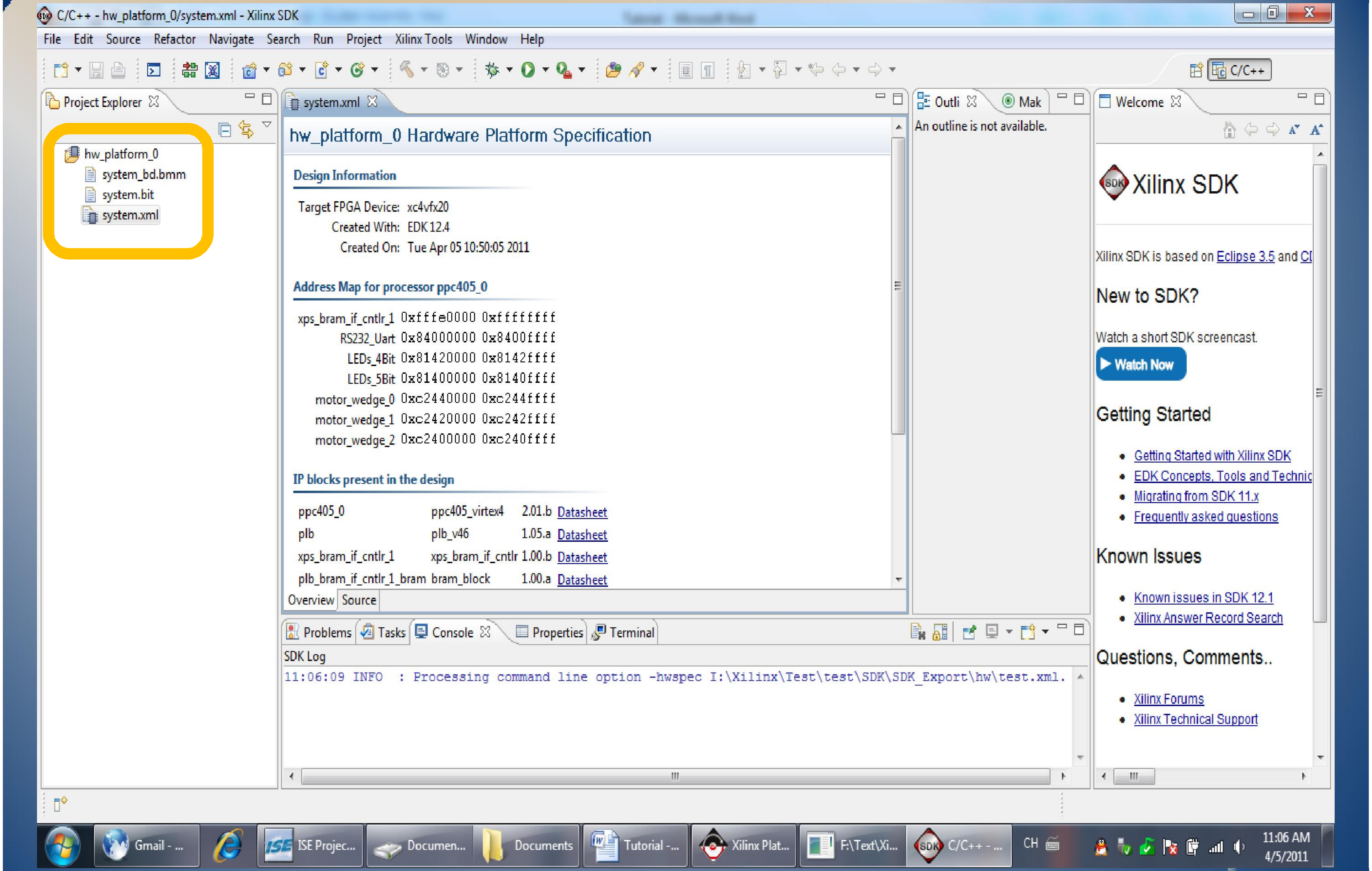
□ Include bitstream and BMM file

(This project has been instantiated in Project Navigator. After exporting to SDK, you must manually copy the bitstream and <design>_bd.bmm file from the Project Navigator directory to the export directory displayed below

Directory location for hardware description files

SDK\SDK_Export

Export to SDK and then Launch SDK



hw_platform_0 Hardware Platform Specification

Design Information

Target FPGA Device: xc4vfx20
Created With: EDK 12.4
Created On: Tue Apr 05 10:50:05 2011

Address Map for processor ppc405_0

```
xps_bram_if_cntlr_1 0xfffe0000 0xffffffff
        RS232_Uart 0x84000000 0x8400ffff
        LEDs_4Bit 0x81420000 0x8142ffff
        LEDs_5Bit 0x81400000 0x8140ffff
      motor_wedge_0 0xc2440000 0xc244ffff
      motor_wedge_1 0xc2420000 0xc242ffff
      motor_wedge_2 0xc2400000 0xc240ffff
```

IP blocks present in the design

ppc405_0	ppc405_virtex4	2.01.b	Datasheet
plb	plb_v46	1.05.a	Datasheet
xps_bram_if_cntlr_1	xps_bram_if_cntlr	1.00.b	Datasheet
plb_bram_if_cntlr_1_bram	bram_block	1.00.a	Datasheet

SDK Log

```
11:06:09 INFO  : Processing command line option -hwspec I:\Xilinx\Test\test\SDK\SDK_Export\hw\test.xml.
```

Xilinx SDK

Xilinx SDK is based on Eclipse 3.5 and CI

New to SDK?

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Getting Started

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- Frequently asked questions

Known Issues

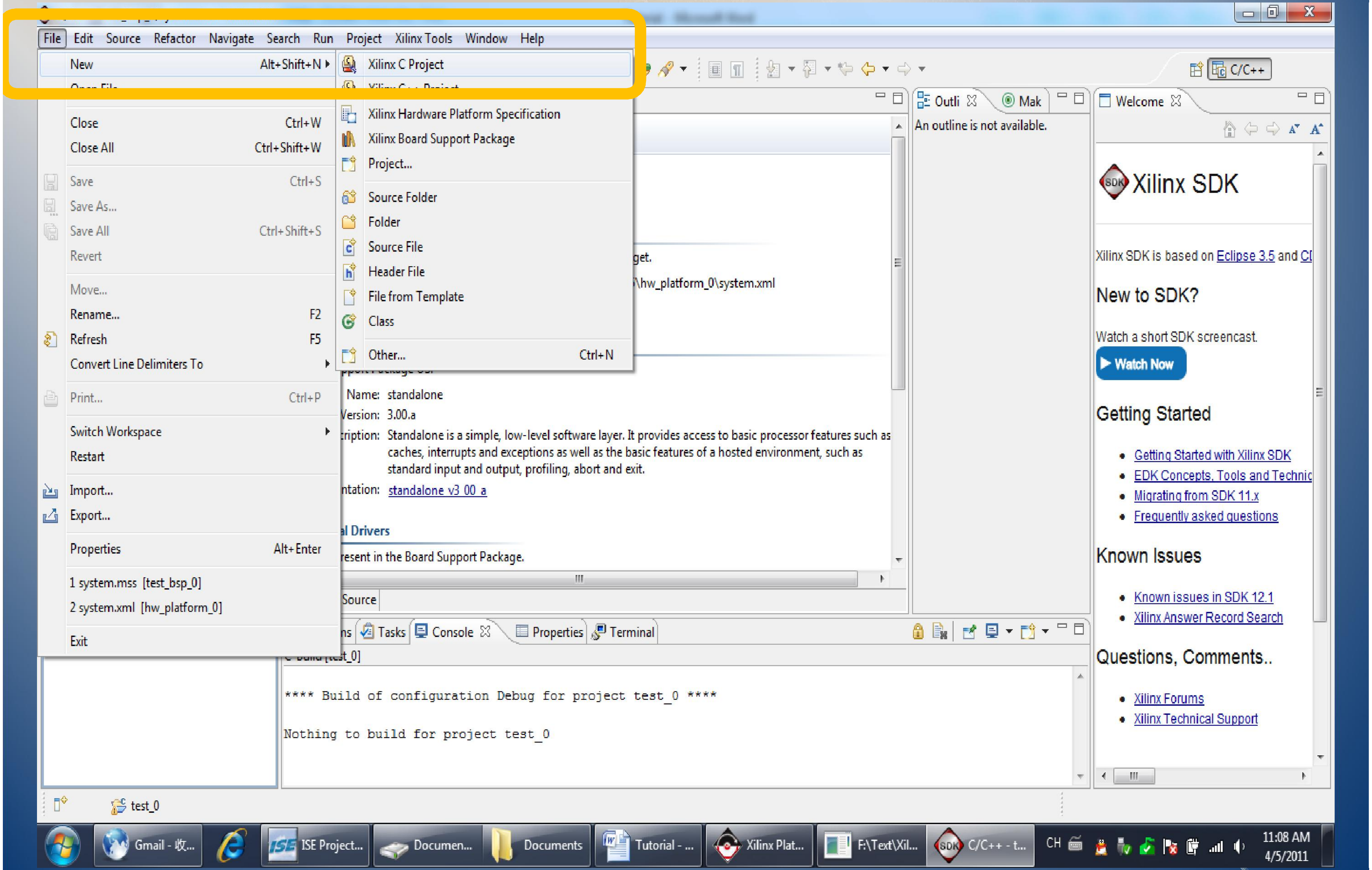
- Known issues in SDK 12.1
- Xilinx Answer Record Search

Questions, Comments..

- Xilinx Forums
- Xilinx Technical Support

Now we opened SDK and there are some files should be automatically generated after we exporting hardware design to it in ISE.

Create a Software Project



An outline is not available.

get.

\hw_platform_0\system.xml

Name: standalone

Version: 3.00.a

ription: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.

ntation: standalone_v3_00_a

l Drivers

resent in the Board Support Package.

```
**** Build of configuration Debug for project test_0 ****

Nothing to build for project test_0
```

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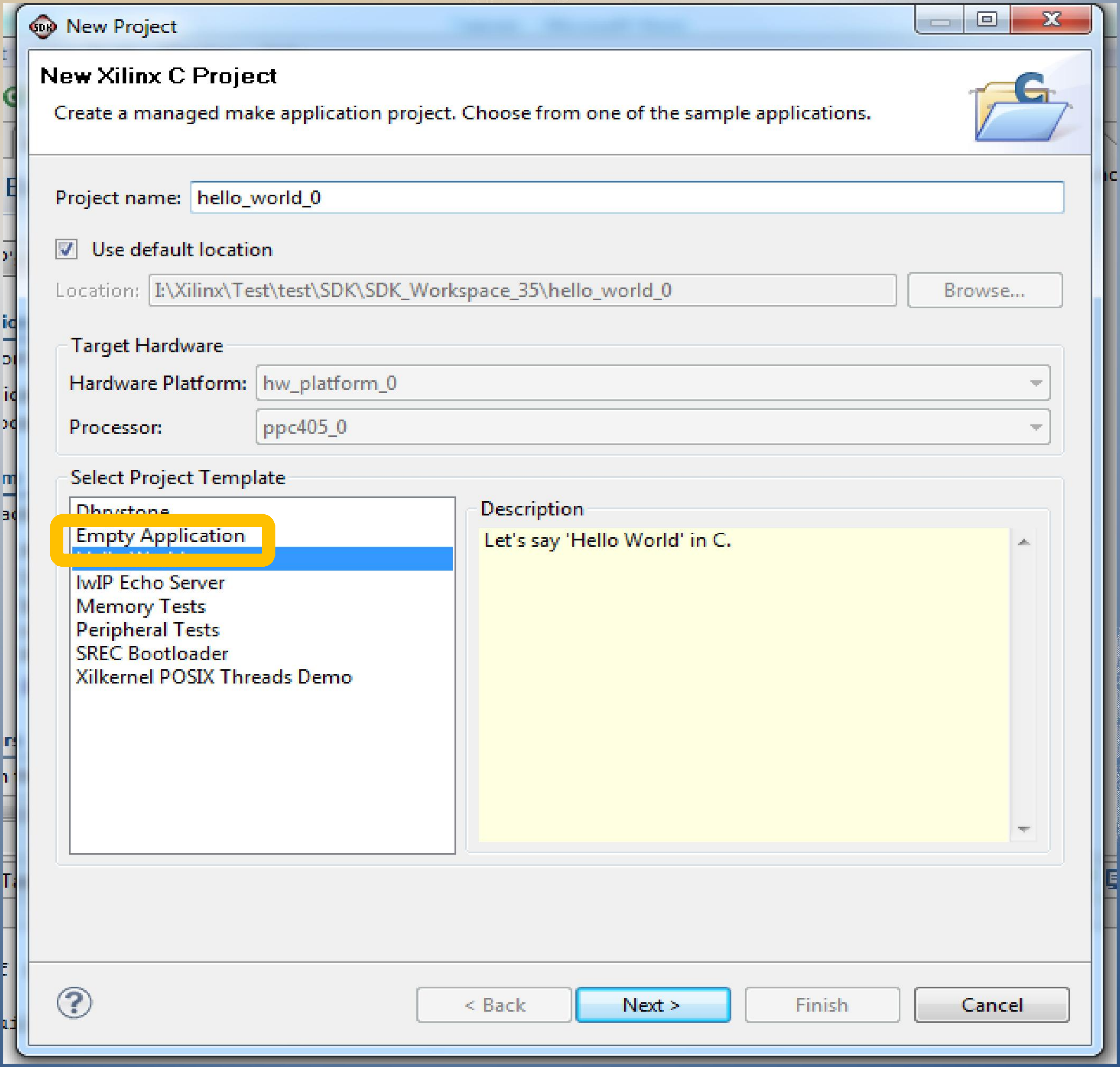


New Project

New Xilinx C Project

Create a managed make application project. Choose from one of the sample applications.

Project name: hello_world_0

☑ Use default location

Location: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hello_world_0

Target Hardware

Hardware Platform: hw_platform_0

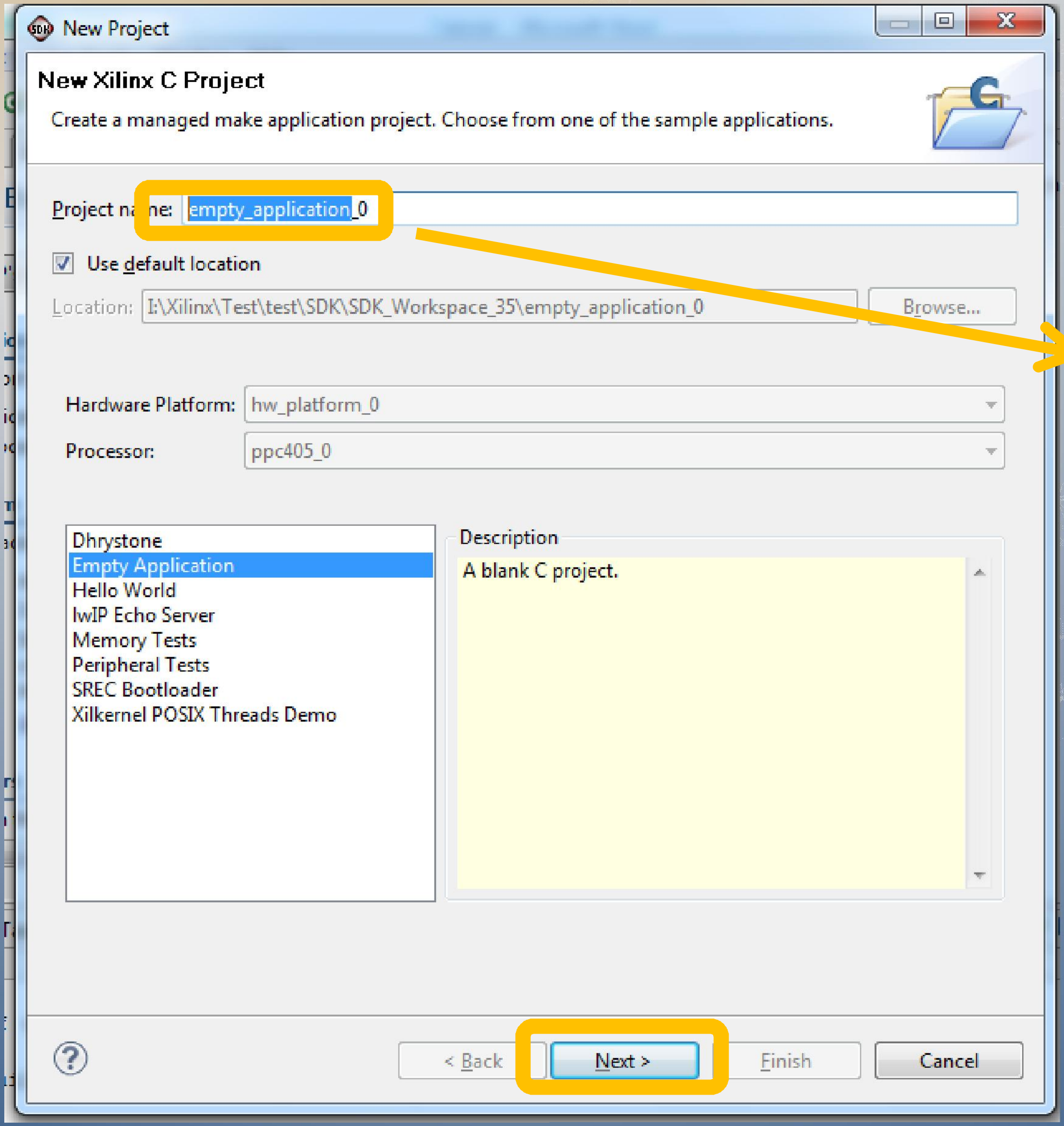
Processor: ppc405_0

Select Project Template

- Dhrystone
- Empty Application
- lwIP Echo Server
- Memory Tests
- Peripheral Tests
- SREC Bootloader
- Xilkernel POSIX Threads Demo

Description

Let's say 'Hello World' in C.



New Xilinx C Project

Create a managed make application project. Choose from one of the sample applications.

Project name: empty_application_0

☑ Use default location

Location: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\empty_application_0

Hardware Platform: hw_platform_0

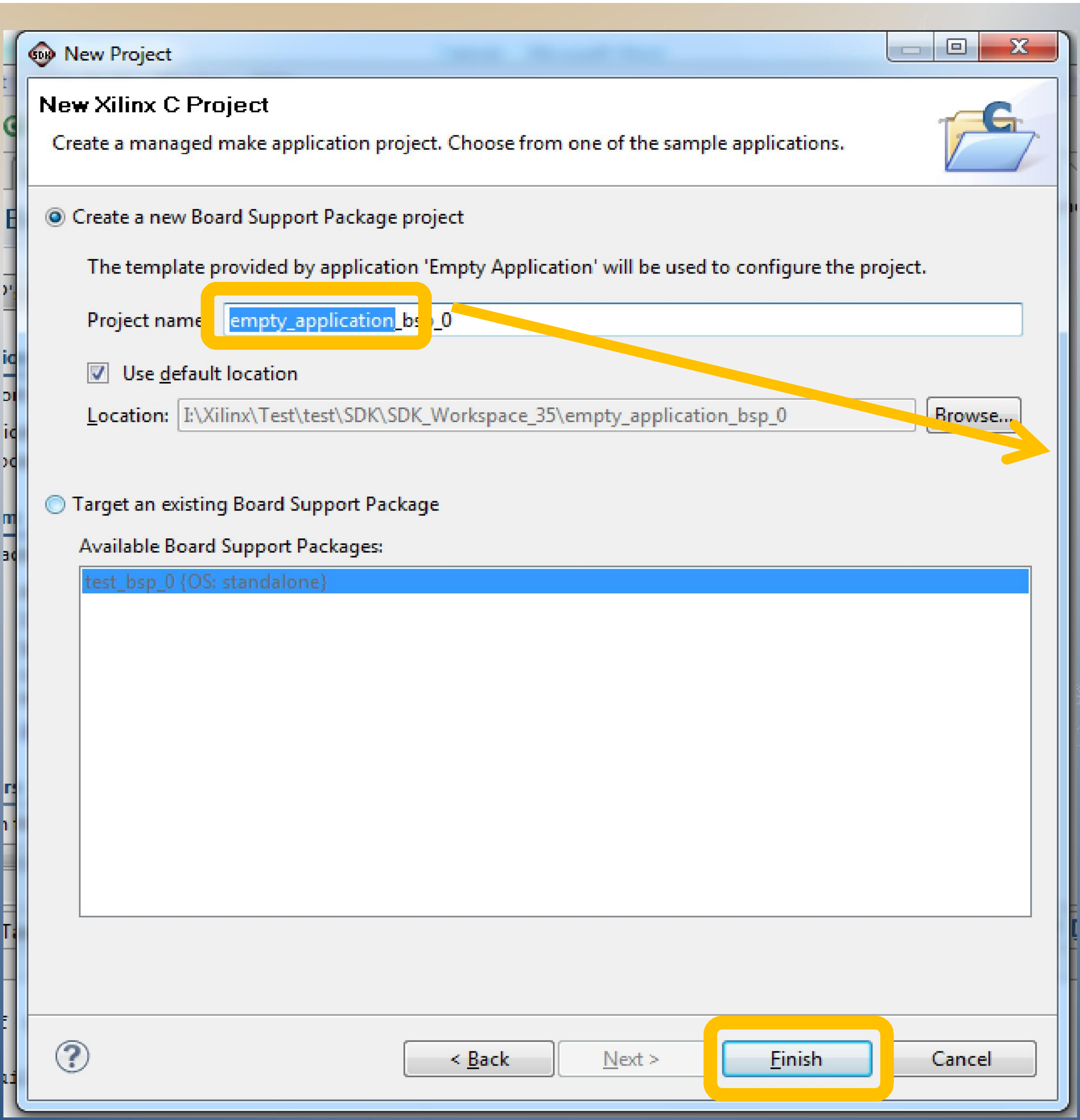
Processor: ppc405_0

- Dhrystone
- Empty Application
- Hello World
- lwIP Echo Server
- Memory Tests
- Peripheral Tests
- SREC Bootloader
- Xilkernel POSIX Threads Demo

Description

A blank C project.

Put the name of the project here.



New Project

New Xilinx C Project

Create a managed make application project. Choose from one of the sample applications.

● Create a new Board Support Package project

The template provided by application 'Empty Application' will be used to configure the project.

Project name: empty_application_bsp_0

☑ Use default location

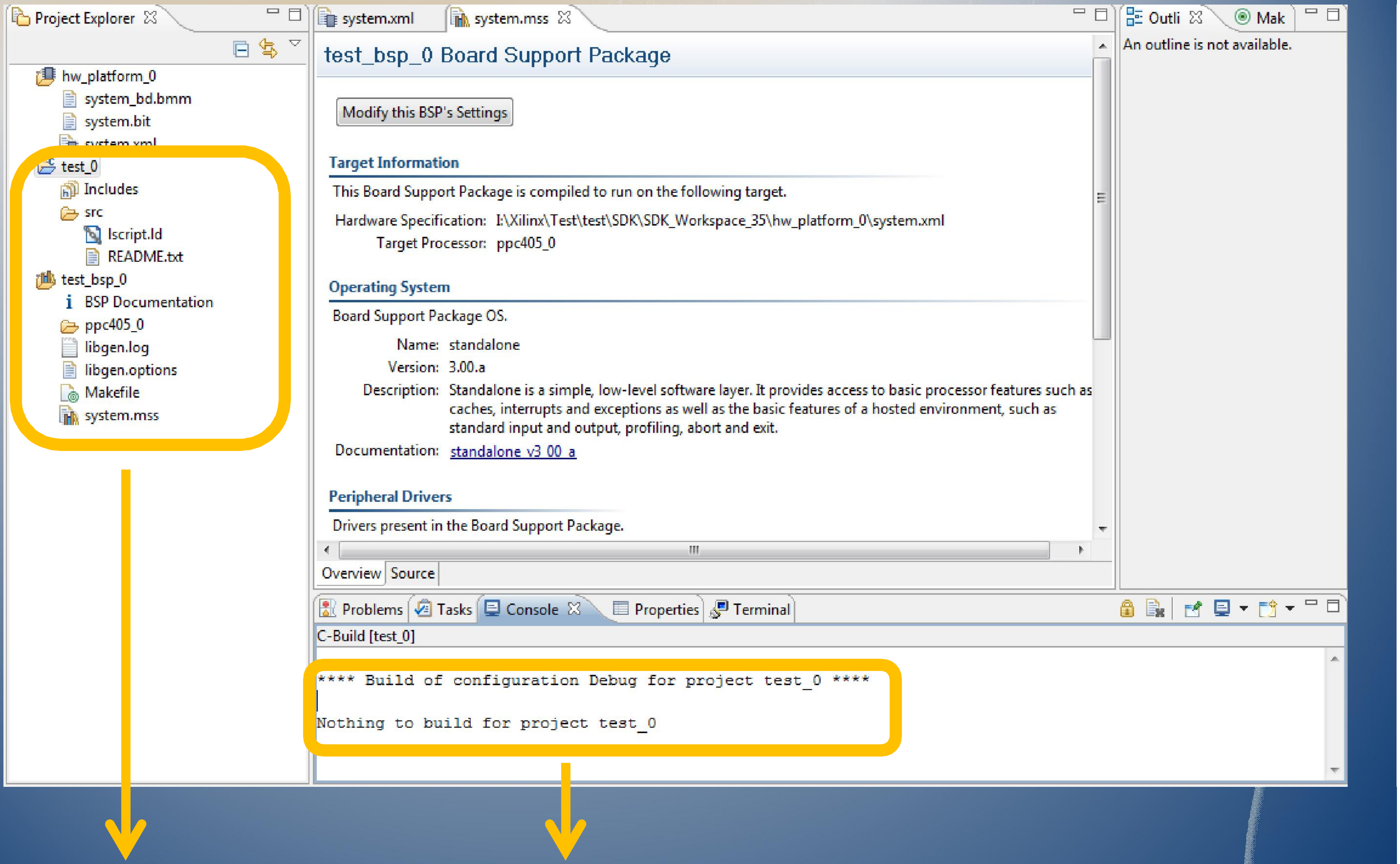
Location: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\empty_application_bsp_0

○ Target an existing Board Support Package

Available Board Support Packages:

test_bsp_0 {OS: standalone}

Same thing. But do leave "_bsp_0 " here.



test_bsp_0 Board Support Package

Target Information

This Board Support Package is compiled to run on the following target.

Hardware Specification: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.xml

Target Processor: ppc405_0

Operating System

Board Support Package OS.

Name: standalone

Version: 3.00.a

Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.

Documentation: standalone_v3_00_a

Peripheral Drivers

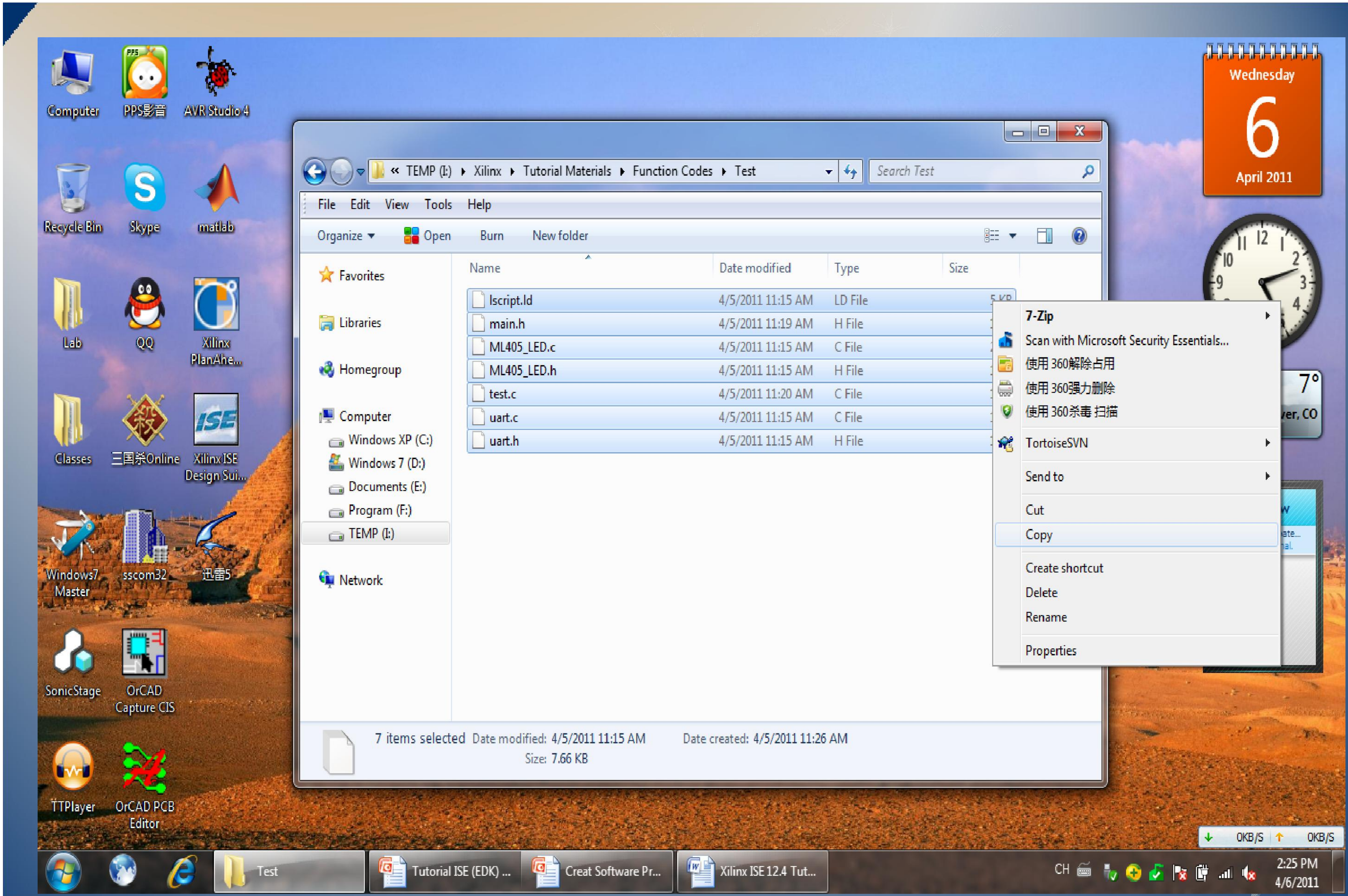
Drivers present in the Board Support Package.

```
**** Build of configuration Debug for project test_0 ****

Nothing to build for project test_0
```

Project we have created.

Wait for the project has been created completely before doing any changes.

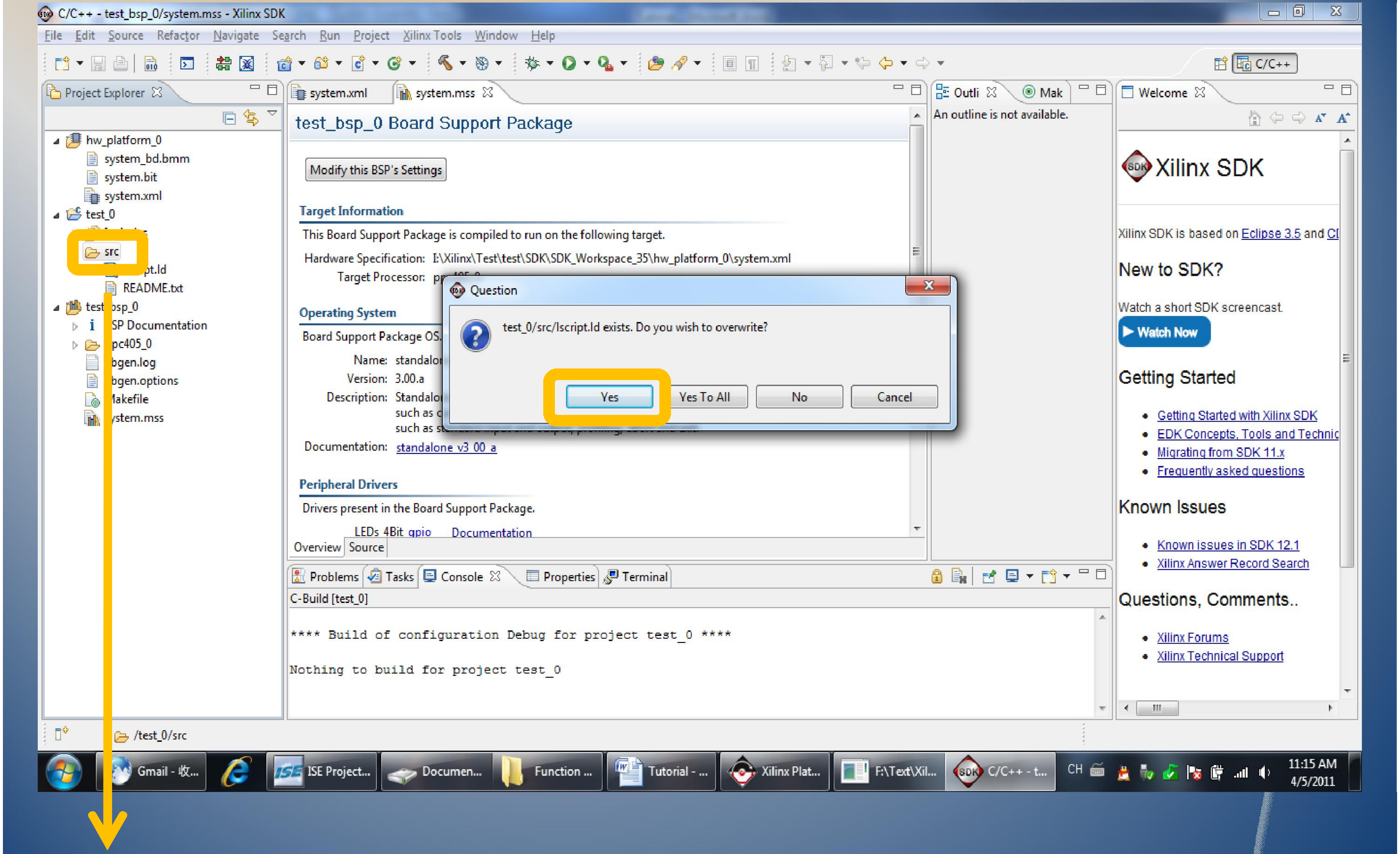


Name	Date modified	Type	Size
lscript.ld	4/5/2011 11:15 AM	LD File	5 KB
main.h	4/5/2011 11:19 AM	H File	
ML405_LED.c	4/5/2011 11:15 AM	C File	
ML405_LED.h	4/5/2011 11:15 AM	H File	
test.c	4/5/2011 11:20 AM	C File	
uart.c	4/5/2011 11:15 AM	C File	
uart.h	4/5/2011 11:15 AM	H File	

7 items selected Date modified: 4/5/2011 11:15 AM Date created: 4/5/2011 11:26 AM

Size: 7.66 KB

Copy the codes under the folder “test” in the “Function Codes” folder.



test_bsp_0 Board Support Package

Modify this BSP's Settings

Target Information

This Board Support Package is compiled to run on the following target.

Hardware Specification: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.xml

Target Processor: pp

Operating System

Board Support Package OS.

Name: standalo

Version: 3.00.a

Description: Standalo such as such as s

Documentation: standalone_v3_00_a

Peripheral Drivers

Drivers present in the Board Support Package.

LEDs_4Bit gpio Documentation

An outline is not available.

Question

test_0/src/lscript.ld exists. Do you wish to overwrite?

Yes | Yes To All | No | Cancel

C-Build [test_0]

```
**** Build of configuration Debug for project test_0 ****

Nothing to build for project test_0
```

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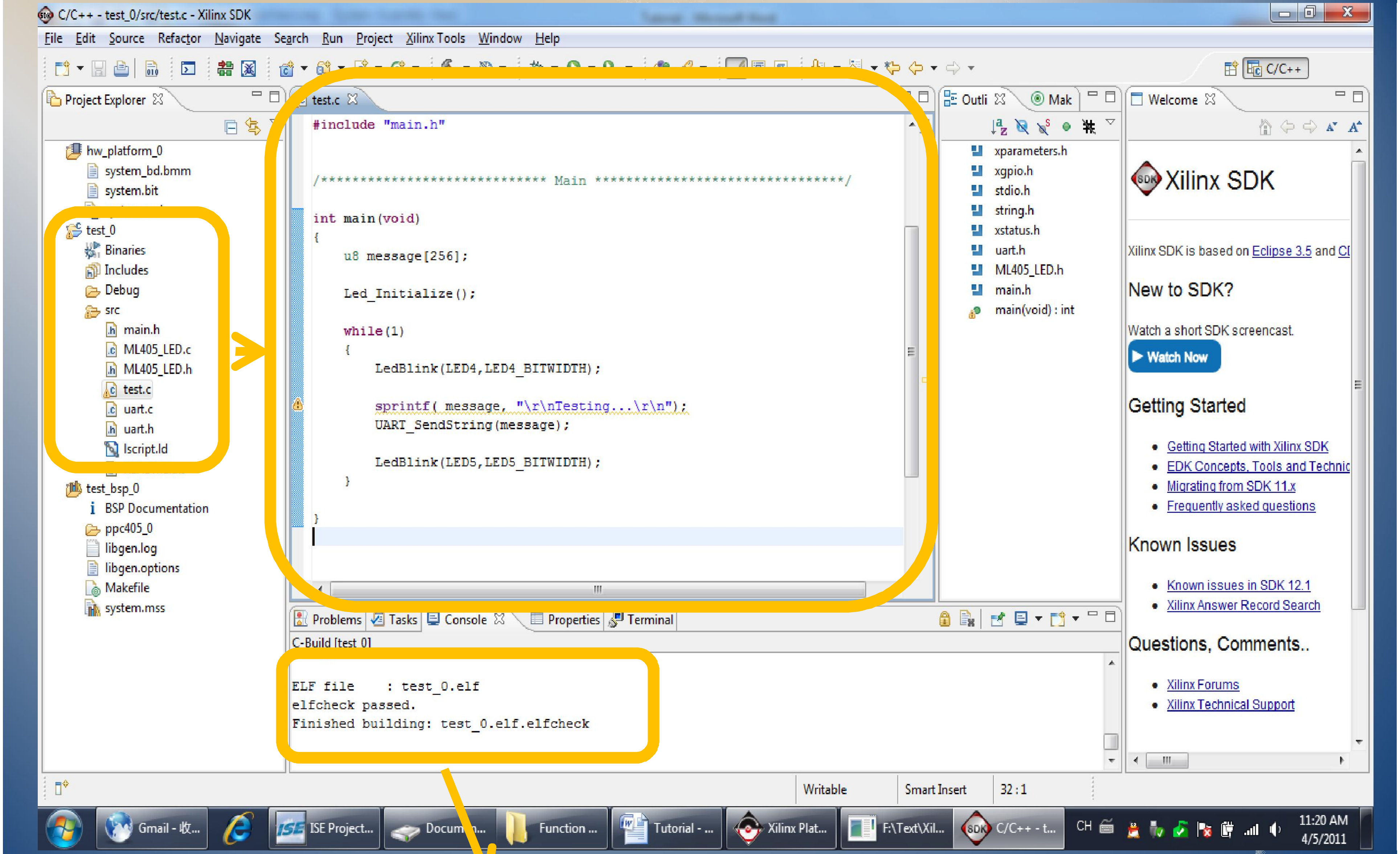
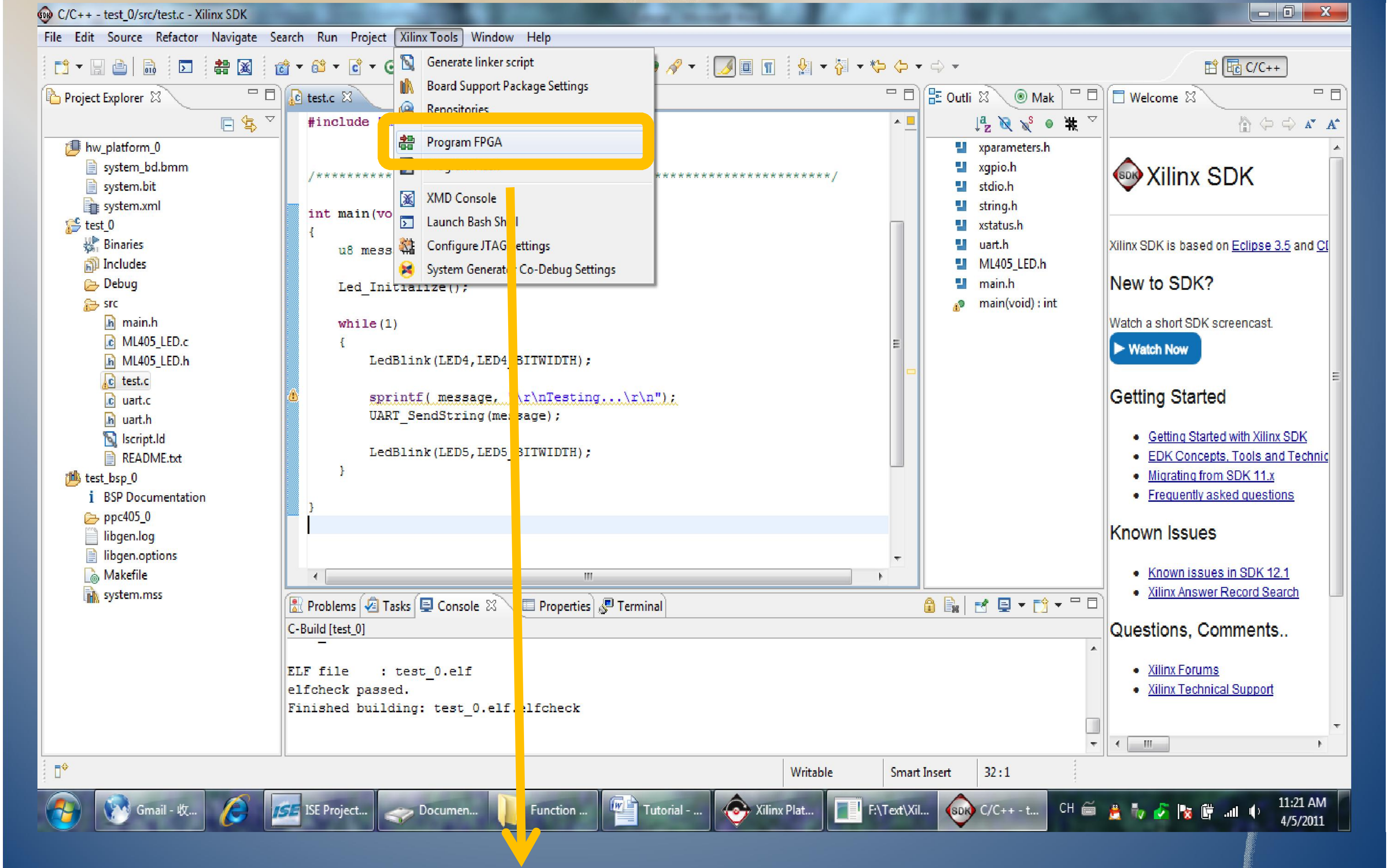
Paste these files here at “src” folder under the C project we built(test_0).



```
#include "main.h"


/****************************** Main *******************************/

int main(void)
{
    u8 message[256];

    Led_Initialize();

    while(1)
    {
        LedBlink(LED4,LED4_BITWIDTH);

        sprintf( message, "\r\nTesting...\r\n");
        UART_SendString(message);

        LedBlink(LED5,LED5_BITWIDTH);
    }

}
```

```
ELF file    : test_0.elf
elfcheck passed.
Finished building: test_0.elf.elfcheck
```

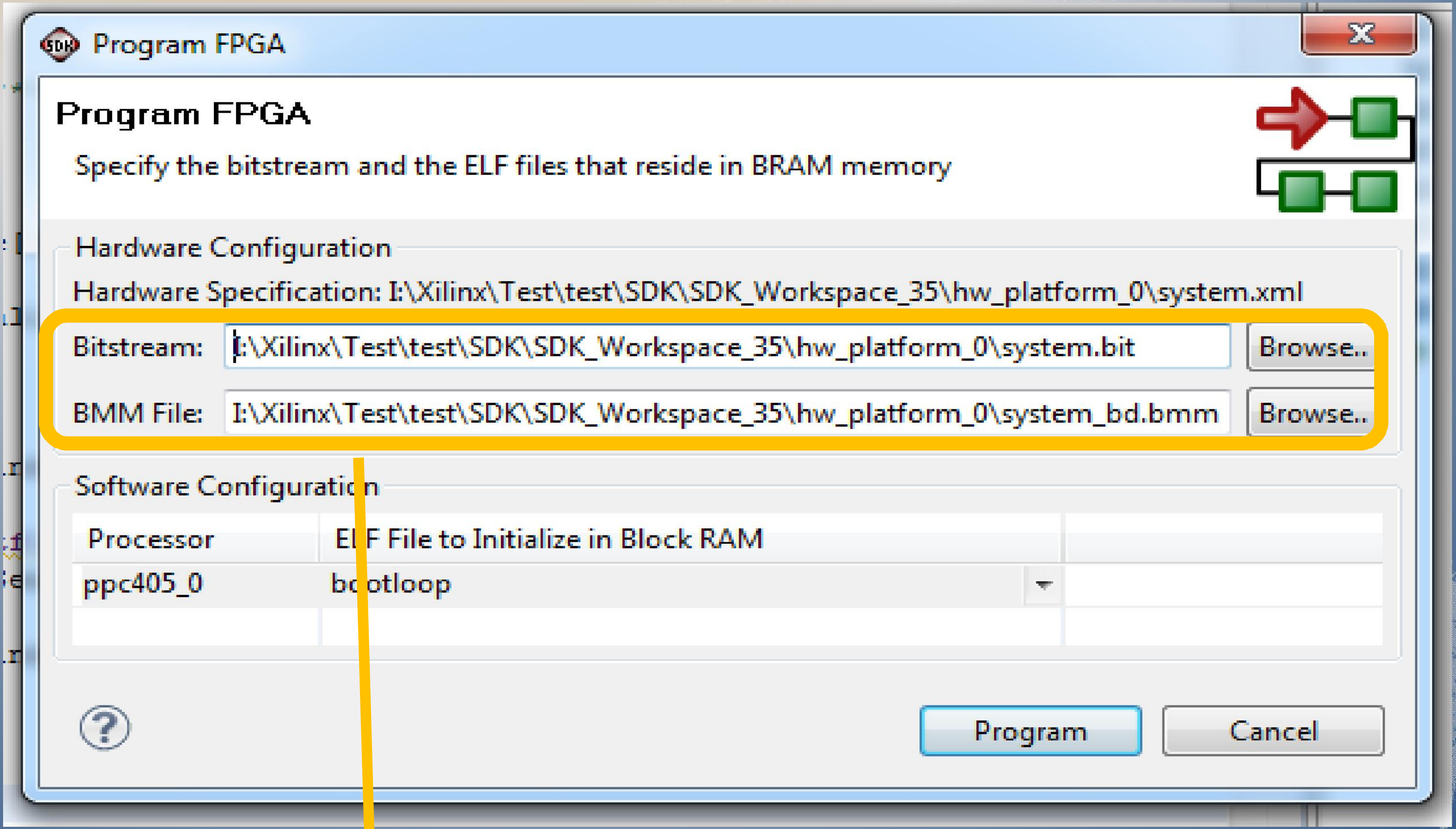
Build the project by saving it or some other ways. We will get .elf file which is to be downloaded into the FPGA.



```
#include
/**********                         ************************/
int main(vo
{
   u8 mess
   Led_Initialize();

   while(1)
   {
      LedBlink(LED4,LED4_BITWIDTH);

      sprintf( message,  \r\nTesting...\r\n");
      UART_SendString(me sage);

      LedBlink(LED5,LED5_BITWIDTH);
   }

}
```

```
C-Build [test_0]

ELF file    : test_0.elf
elfcheck passed.
Finished building: test_0.elf.elfcheck
```

Download our project into the FPGA by this option.



Program FPGA

Specify the bitstream and the ELF files that reside in BRAM memory

Hardware Configuration

Hardware Specification: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.xml

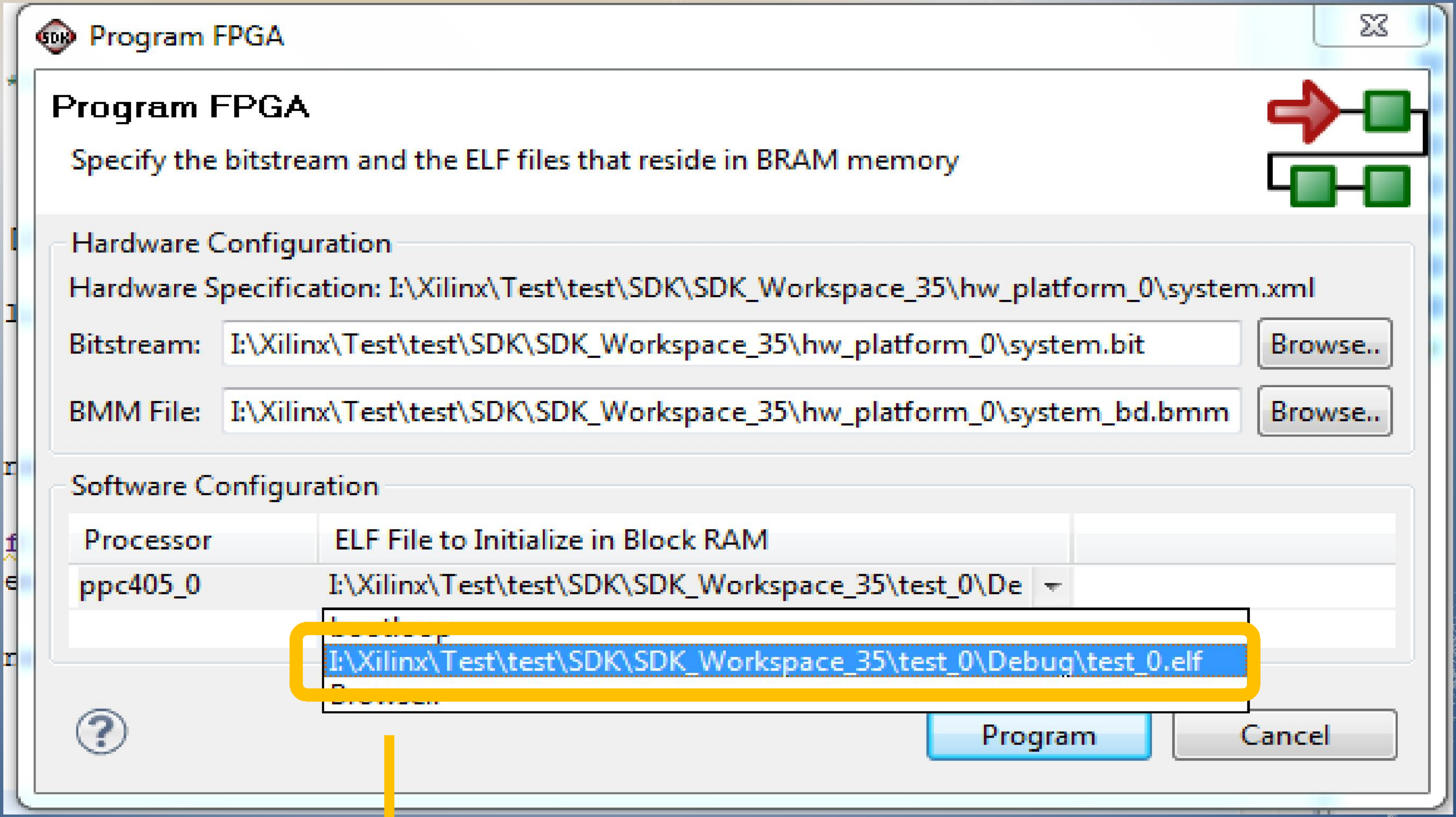
Bitstream: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.bit

BMM File: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system_bd.bmm

Software Configuration

Processor	ELF File to Initialize in Block RAM
ppc405_0	bootloop

These two file should be generated automatically .



Program FPGA

Specify the bitstream and the ELF files that reside in BRAM memory

Hardware Configuration

Hardware Specification: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.xml

Bitstream: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.bit

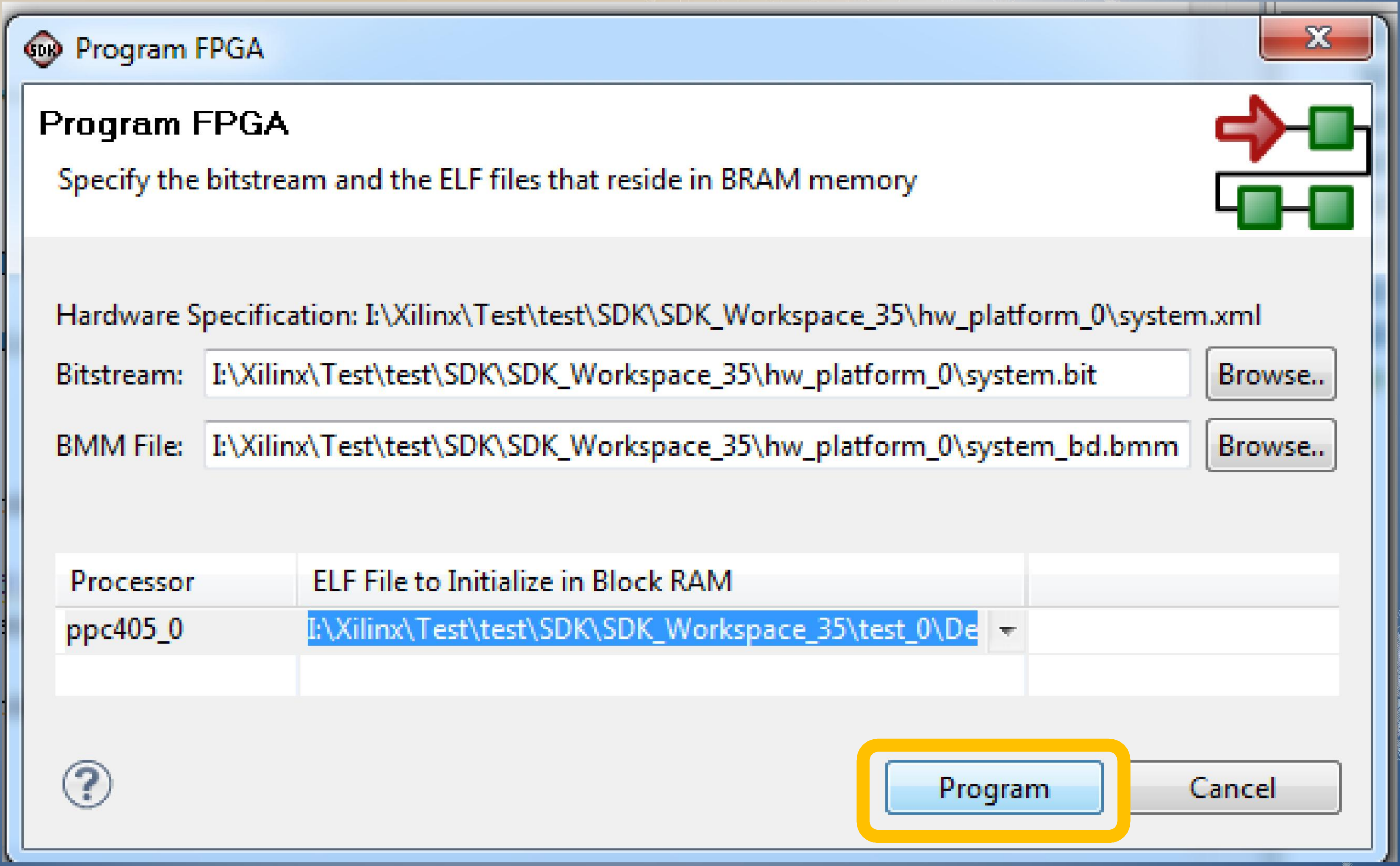
BMM File: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system_bd.bmm

Software Configuration

Processor	ELF File to Initialize in Block RAM
ppc405_0	I:\Xilinx\Test\test\SDK\SDK_Workspace_35\test_0\De

I:\Xilinx\Test\test\SDK\SDK_Workspace_35\test_0\Debug\test_0.elf

The .elf file is what we are going to download into FPGA.



Program FPGA

Program FPGA

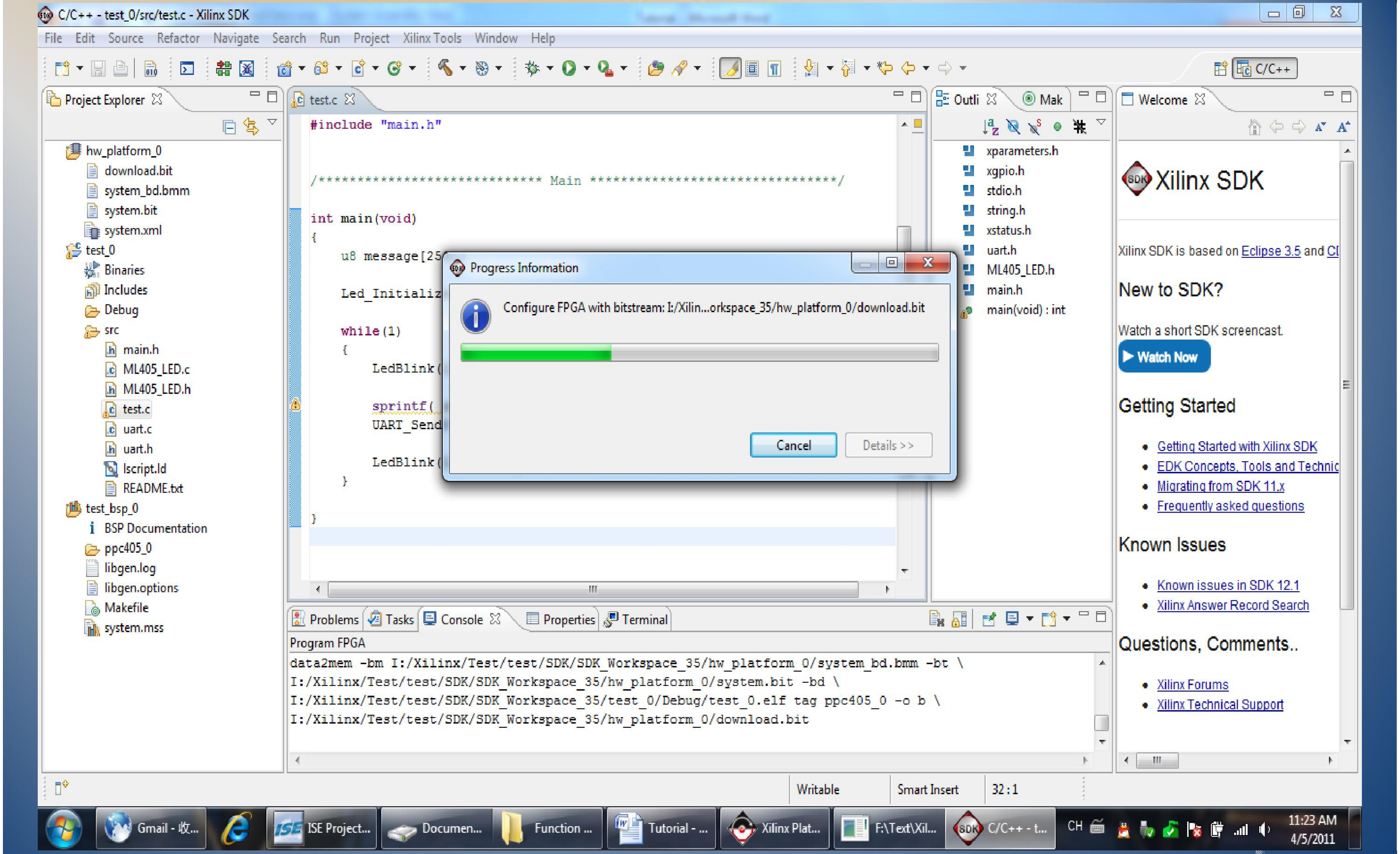
Specify the bitstream and the ELF files that reside in BRAM memory

Hardware Specification: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.xml

Bitstream: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.bit

BMM File: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system_bd.bmm

Processor	ELF File to Initialize in Block RAM
ppc405_0	I:\Xilinx\Test\test\SDK\SDK_Workspace_35\test_0\De



```
#include "main.h"

/***************************** Main ********************************/

int main(void)
{
    u8 message[25
    Led_Initializ
    while(1)
    {
        LedBlink(
        sprintf(
        UART_Send
        LedBlink(
    }
}
```

Progress Information

Configure FPGA with bitstream: I:/Xilin...orkspace_35/hw_platform_0/download.bit

Cancel Details >>

Program FPGA

```
data2mem -bm I:/Xilinx/Test/test/SDK/SDK_Workspace_35/hw_platform_0/system_bd.bmm -bt \
I:/Xilinx/Test/test/SDK/SDK_Workspace_35/hw_platform_0/system.bit -bd \
I:/Xilinx/Test/test/SDK/SDK_Workspace_35/test_0/Debug/test_0.elf tag ppc405_0 -o b \
I:/Xilinx/Test/test/SDK/SDK_Workspace_35/hw_platform_0/download.bit
```

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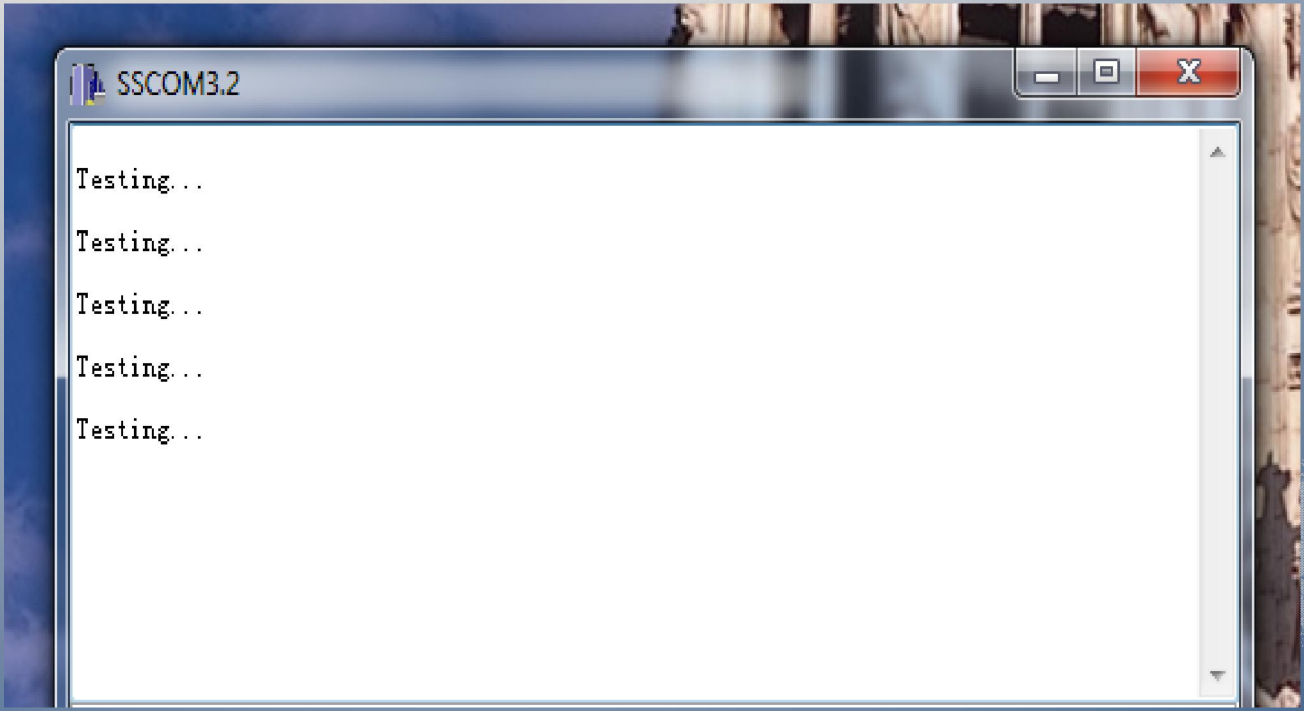
Downloading.

Result

First, two sets of LEDs on the ML405 should be blinking. Then some message should be sent through UART to your PC.



```
Testing...

Testing...

Testing...

Testing...

Testing...
```

Open your hyper-terminal or something like it. Chose the com you connected and set Baud Rate as 9600. Details about it can be found in the property of the uart IP core in XPS.