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## Part I: ISE12.4 Installation

Download ISE12.4 on Xilinx Webpage:

http://www.xilinx.com/support/download/index.htm

Design Too	S Device Models CAE Vendor Libraries			
Version	ISE Design Suite - 12.4 Full Product Installation			*
13.1	All Platforms (TAR/GZ - 4.39 GB) MD5 Sum Value: eb743b99096e39a8996d8ee8e673b486	Download Includes	ISE WebPACK (Free) ISE Design Suite (All Editions)	
12.4 12.3	Full Installer for Windows (TAR/GZ - 3.38 GB) MD5 Sum Value: 9aab55db13d0b5aaa6b375856421ec20	]	ChipScope Pro and ChipScope Pro Serial IO Toolkit PlanAhead Design and Analysis	
12.2	Full Installer for Linux (TAR/GZ - 3.48 GB) MDC Cum Method 225022C-2-6677 (2004084-8-0-00444)		System Generator for DSP Platform Studio and Embedded Development Kit (EDK)	
12.1	MD5 Sum Value: 3309326836175126906618689809104	Devueland Trees	Software Development Kit (SDK) Lab Tools: Standalone Installation	
11.5		Last Updated Enablement	12/21/2010 License Solution Center	
11.3		Order DVD	ISE Design Suite DVD	Ш

#### ISE Design Suite 12.4 Installer



### Welcome

We are glad you've chosen Xilinx as your platform development partner. This program will install ISE WebPACK, one of the four ISE Design Suite Editions or one of our two standalone products. The installation process will consist of the steps listed to the left.

You will need to have administrator privileges in order to install this software on Windows operating systems. To reduce installation time, we recommend that you disable any anti-virus software before continuing.

For the product you select to install, we also recommend that you install to a new directory. If you choose to install your selected product into a directory with an older installation of ISE Design Suite, we will require the older version to be uninstalled before proceeding.

#### ISE Design Suite 12.4 Installer

#### -> Welcome

Accept License Agreements Select Edition to Install Select Installation Options Select Destination Directory Installation

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Cancel

## Install Mainpage-----Click Next

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	Select Edition to Install
XILINX.	<ul> <li>Edition List</li> </ul>
	ISE WebPACK
	ISE Design Suite: Logic Edition
DESIGN SUITE	ISE Design Suite: Embedded Edition
	ISE Design Suite: DSP Edition
	ISE Design Suite: System Edition
	Software Development Kit: Standalone Installation
	Lab Tools: Standalone Installation
SE Design Suite 12.4 Installer	
Welcome Accept License Agreements -> Select Edition to Install Select Installation Options Select Destination Directory Installation	Disk Space Required : 9956 MB Description of ISE Design Suite: Embedded Edition ISE Design Suite: Embedded Edition contains everything you need to do a complete embedded design. Embedded Edition includes ISE Design Suite Logic Edition plus the Embedded Development Kit (EDK). EDK includes Xilinx Platform Studio (XPS), Software Development Kit (SDK), and Embedded IP.
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This step has a trick: Please choose Embedded Edition, then Click Next and Begin Install

	Xilinx License Cor	figuration Manager	
	Acquire a License	Manage Xilinx Licenses	
	-Select one of the	following options	
	Start Now! -	30 Day Trial (No Bitstream)	
	Start ISE We	bPack	
	Start 30 Day	Evaluation	
	Get My Purch	ased License(s)	
*	Ocate Existing	ng License(s)	
After Installation,	-Description of the	above selected option	
you should make the	This selection wil	l open the "Manage Xilinx Licenses" tab. On this tab, you can copy an existing Xilinx license file to the default o	directory, or you
Liconso			
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Xilinx License Configura	tion Manager	A College Contraction of the second	
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Instructions: Xilinx applic button to copy a license	ations automatically file into this directory	detect valid, node-locked licenses (*.lic) residing in the local .Xilinx directory. U ,	ise the Copy License
To point to a floating ser users will need to make t 1234@server:/usr/local/	ver license, or to poi hese settings outside 'flexlm (Linux)	nt to license files in locations other than .Xilinx, set one of the environment var e of this application.) Examples: 1234@server;C:\licenses\Xilinx.lic (Windows)	riables below, (Linux or
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LM_LICENSE_FILE	2100@130.253.4.1	30	<u>S</u> et

One the blank row, input 2100@130.253.4.130 This is license Dr. Voyles bought for CML.

After License Configuration, you can try ISE 12.4 according to the next part tutorial



# Part II: Create a Project in ISE 12.4

This tutorial will show you how to recreate a project in EDK with some files in the folder.

Part 1 is about creating a new project in ISE.

Part 2 is about adding IPs cores to the project in the XPS, including the IPs xilinx provided and IPs user created.

Part 3 is about creating software projects in the SDK, writing codes and downloading them into the FPGA.

SE Project Navigator (M.81d)		
Edit View Project Source Process Tools Window Lavout Help		
Welcome to the IEF® Decise Cuite		
roject commands		
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ouble click on a project in the list below to open		
Test_EDK_LED		
Test_3Motor_Wedge_2		
Test	Chart	
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ISE Design Suits Info@estar		
Key New Features in Project Navigator	Welcome to the ISE@ Design	Suito
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m		
Console 🔕 Errors 🔔 Warnings 😿 Find in Files Results	Pecent projects	
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	Double click on a project in the list below to open	
	Test_EDK_LED	<b>A</b>
	Test_cc2520	
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	Test_3Motor_Wedge 2	
	Tert	<b>T</b>
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		#

С	New Project reate New Project	Wizard	
Sp	ecify project location Enter a name, location N <u>a</u> me: Location: Working Directory: Description:	and type. ons, and comment for the project I:\vilinx I:\vilinx Type the name of the project, for example, "Test"	
	Select the type of to <u>T</u> op-level source typ HDL	p-level source for the project e:	

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### New Project Wizard

## Project Settings

Specify device and project properties. Select the device and design flow for the project -

Property Name	Value	
Product Category	All	•
Family	Virtex4	•
Device	XC4VFX20	•
Package	FF672	-
Speed	-10	•
Top-Level Source Type	HDL	Ŧ
Synthesis Tool	XST (VHDL/Verilog)	•
Simulator	ISim (VHDL/Verilog)	•
Preferred Language	VHDL	•
Property Specification in Project File	Store all values	•
Manual Compile Order		
VHDL Source Analysis Standard	VHDL-93	-
Enable Message Filtering		

X

```
23
G
        New Project Wizard
  Project Summary
  Project Navigator will create a new project with the following specifications.
  Project:
      Project Name: Test
      Project Path: I:\Xilinx\Test
      Working Directory: I:\Xilinx\Test
      Description:
      Top Level Source Type: HDL
  Device:
      Device Family: Virtex4
      Device:
                    xc4vfx20
                                                                                 E
      Package: ff672
      Speed:
                    -10
      Synthesis Tool: XST (VHDL/Verilog)
      Simulator: ISim (VHDL/Verilog)
      Preferred Language: VHDL
      Property Specification in Project File: Store all values
      Manual Compile Order: false
      VHDL Source Analysis Standard: VHDL-93
      Message Filtering: disabled
                                                               Finish
                                                                          Cancel
  More Info
```



📧 New Source Wizard		
Select Source Type Select source type, file name and its location. P (CORE Generator & Architecture Wizard) Schematic User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Library VHDL Dackage VHDL Test Bench Embedded Processor	Eile name: test Location: I:\Xilinx\Test	
More Info	☑ <u>A</u> dd to project	Next Cancel

G	New Source Wizard
	Summary
,	Project Navigator will create a new skeleton source with the following specifications.
	Add to Project: Yes
	Source Type: Embedded Processor
	Source Name: test.xmp
	EDK will be launched to allow you to configure your new processor design.
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## Part III: Add IP cores in XPS

This part will show you how to add IP cores in XPS. Several IPs will be added, including a LEDs\_4Bit IP, a general purpose IO IP, and three MOTOR\_WEDGE IP.



Welcome	Board	System	Processor	Peripheral	Cache	Application	Summary
ome to the Base	System Builder						
s tool leads you throug	gh the steps neces	sary for creating	an embedded syste	m.			
ect One of the Follow	ing:						
I would like to create	e a new design	ttings file (saved	from a previous ses	sion)			
	in existing itsis se	cango nie (ouveu	n on a previous ses	siony			Browse
							bromac m

welcome	Board	System	Processor	Peripheral	Cache	Application	Summary
ard Selection							
ect a target devel	opment board.						
ard							
I would like to cr	eate a system for the	e following develo	pment board				
Board Vendor	Xilinx						-
Board Name	Virtex 4 ML405 Eval	uation Platform					•
Board Revision	1						•
I would like to cr	eate a system for a d	custom board					
ard Information	n.						
- hitecture	De	vice	Da	ckage	Spi	eed Grade	
rtex4	- X0	:4vfx20		672	▼ -1	0	
Use Stepping							
set Polarity Activ	elow						
ated Information							
della contrata C							
ndor's Contact Info	ormation						
rd Party Board De	finition Files Downloa	d Website					
e ML405 board is ir izes Yiliny Virtey 4	tended to showcase	and demonstrate	Virtex-4 technology	, especially the new f	eatures being add	ed to the FPGA. The vibility of Virtex-4 EPC	ML405 board
w and improved do	ock technology, DSP	blocks, Smart RAM	blocks, advanced I/	Os, embedded MACs	, embedded proce	ssors, Multi Gigabit Tr	ansceivers
GT), and more. Ple	ase reference AR23	410 for MGT issue	on this board.				



cessor Configuration   figure the processor(s).	Essor Configuration pure the processor (s). ence Clock Frequency 100.00 cessor 1 Configuration cessor Type PowerPC cessor Clock Frequency 100.00 V Hriz clock Frequency 100.00 V Hriz clock Frequency 100.00 V Hriz cassor Type PowerPC Cessor Clock Frequency 100.00 V Hriz cessor Frequency 100.00	Welcome Be	oard	System	Processor	Peripheral	Cache	Application	Summary	C F
hfigure the processor (s).	pure the processor (s).  ence Clock Frequency 100.00  MHz cessor 1 Configuration  cessor Type PowerPC  cessor Clock Frequency 100.00  MHz clock Frequency 100.00  MHz chip Memory None  nug Interface FPGA JTAG  Enable Floating Point Unit	ocessor Configuration								
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Processor 1 Configuration         Processor Type       PowerPC         Processor Clock Frequency       100.00         Sus Clock Frequency       100.00         On-chip Memory       None         Debug Interface       FPGA JTAG         Image: Enable Floating Point Unit       2	cessor 1 Configuration cessor Type PowerPC cessor Clock Frequency 100.00 MHz clock Frequency 100.00 MHz chip Memory None rug Interface FPGA JTAG Enable Floating Point Unit 2	eference Clock Frequency	100.00						MHz	
Processor Type PowerPC   Processor Clock Frequency 100.00   Bus Clock Frequency 100.00   On-chip Memory None   Debug Interface FPGA JTAG   Enable Floating Point Unit 2	cessor Type       PowerPC         cessor Clock Frequency       100.00         clock Frequency       100.00         chip Memory       None         cug Interface       PPGA JTAG         Enable Floating Point Unit       2	Processor 1 Configuration —								
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On-chip Memory None     Debug Interface     FPGA JTAG     Enable Floating Point Unit	-chip Memory None   Dug Interface FPGA JTAG   Enable Floating Point Unit	Bus Clock Frequency	100.00						▼ MHz	
Debug Interface FPGA ITAG v	Enable Floating Point Unit	On-chip Memory	None						•	
Enable Floating Point Unit	Enable Floating Point Unit	Debug Interface	FPGA JTAG						-	

Available Peripherals       Peripheral Names       Image: Display and the second	Processor 1 (PowerPC 405)		
FLASH	Core	Parameter Parameter	
⊡Internal Peripherals xps_bram_if_cntlr xps_timebase_wdt xps_timer	Core         Ethernet_MAC         Core: xps_ethernetlite         IIC_EEPROM         Core: xps_jiic         LEDs_4Bit         Core: xps_gpio         LEDs_Positions         Core: xps_gpio         MGT_wrapper         Core: xps_gpio         Remove         Remove         SRAM         Core: xps_uartlite, Ba         SRAM         Core: xps_wratlite, Ba         SRAM         Core: xps_mch_emc         SysACE_CompactFlash         Core: xps_sysace         xps_bram_if_cntlr_1         Core: xps_bram_if_cnt	Processor 1 (PowerPC 405) Peripherals Core LEDs_4Bit Core: xps_gpio RS232_Uart Core: xps_uartlite, Baud Rate: 9600, D xps_bram_if_cntlr_1 Core: xps_bram_if_cntlr, Size: 8 KB th, Size: 8 KB Remove or	Select Al Parameter

Welcome Boa	ard System	Processor	Peripheral	Cache	Application	Summary
e Configuration						5
t cache size and cache mem	nory for processor(s).					
cessor 1 (PowerPC 405) Ca	ache					
e PowerPC embedded in the Itiple memory regions.	e Virtex4FX series of FPG	As provides 16K of	caches. Caches are enable	ed in software,	and can be configure	d to cache
Instruction Cache			Data Cache			In
struction Cache Size 16 K	В	-	Data Cache Size 16 KE	3		<b>v</b>
struction Cache Memory			Data Cache Memory			
xps_oram_ir_cnur_i			xps_pram_ir_criti	II_I		

Welcome B	oard System	Processor	Peripheral	Cache	Application	Summary
Application Configuration	tions.					
Example Applications						
Application	Option Va	lue				
E Test ppc405_0						
Standard IO	RS232_Ua	rt				<b>v</b>
Boot Memory	xps_bram	_if_cntlr_1				<b>T</b>
Memory Test	TestApp_N	/lemory_ppc405_0				
Instructions	xps_bram	_if_cntlr_1				<b>*</b>
- Data	xps_bram	_if_cntlr_1				<b>T</b>
Peripheral Test	TestApp_F	eripheral_ppc405_0				
Instructions	xps_bram	_if_cntlr_1				<b>_</b>
··· Data	xps_bram	_if_cntlr_1				<u> </u>
Interrupt Vecto	r No Interru	ıpt				<b>_</b>

Summary Below is the summary of the system you are creating.  ystem Summary Core Name Instance Name Base Address High Address  Processor1 ppc405_0 xps_gpio LEDs_4Bit 0x81400000 0x8140FFFF xps_uartite R5232_Uart 0x84000000 0x8400FFFF xps_bram_if_cntlr_1 0xFFFFE000 0xFFFFFFFF xps_bram_if_cntlr xps_bram_if_cntlr_1 0xFFFFE000 0xFFFFFFFF  PXUInxXTestVestVestItest.xmp PXXIInxXTestVestVestItest.ucf PXXIInxXTestVestVestVestVest_untime.opt PXXIInxXTestVestVestVestVest_Untime.opt PXXIInxXTestVestVestVestVestUpen.ut PXXIInxXTestVestVestVestUpen.ut PXXIInxXTestVestVestVestUpen.ut PXXIInxXTestVestVestVestUpen.ut PXXIInxXTestVestVestVestVestUpen.ut PXXIInxXTestVestVestVestVestVestVestVestVestVestV			iem moe	essor P	eripnerai	Cache	Application	Summary	
System Summary Core Name Instance Name Base Address High Address Core Name Instance Name Base Address High Address Processor1 ppc405_0 xps_gpio LEDs_4Bit 0x81400000 0x8140FFF xps_uartlite R5232_Uart 0x8400000 0x8400FFF xps_bram_if_cntlr xps_bram_if_cntlr_1 0xFFFFE000 0xFFFFFFF	<b>Summary</b> Below is the summary of th	ne system you are crea	ting.						
Core Name       Instance Name       Base Address       High Address            Processor 1	ystem Summary	10 SV							
Processor 1 ppc405_0 xps_gpio LEDs_4Bit 0x8140000 0x8140FFFF xps_uartlite RS232_Uart 0x8400000 0x8400FFFF xps_bram_if_cntlr xps_bram_if_cntlr_1 0xFFFFE00 0xFFFFFFFF ile Location Overall I Xilinx/Test/test/test.mps I Xilinx/Test/test.mps I Xilinx/Test/test.mas I Xilinx/Test.mas I Xilinx/Test.mas I Xilinx/Test.mas I Xilinx/Test.mas I Xilinx/Test.	Core Name	Instance Name	Base Address	High Addres	s				
File Location  Overall  II:Xilinx\Test\test\test.xmp I:Xilinx\Test\test\test.mss I:Xilinx\Test\test\test.mss I:Xilinx\Test\test\test.ucf I:Xilinx\Test\test\test_runtime.opt I:Xilinx\Test\test\test\test\test\test_etc\download.cmd I:Xilinx\Test\test\test\test\test\test\test.ms I:Xilinx\Test\test\test\test\test_etc\download.cmd I:Xilinx\Test\test\test\test\test\test\test.ms I:Xilinx\Test\test\test\test\test.ms I:Xilinx\Test\test\test\test\test.ms I:Xilinx\Test\test\test\test.ms I:Xilinx\Test\test\test\test\test.ms I:Xilinx\Test\test\test\test\test.ms I:Xilinx\Test\test\test\test.ms I:Xilinx\Test\test\test\test.ms I:Xilinx\Test\test\test\test\test.ms I:Xilinx\Test\test\test\test\test.ms I:Xilinx\Test\test\test\test\test\test\test.ms I:Xilinx\Test\test\test\test\test\test\test\test	rocessor1 xps_gpio xps_uartlite xps_bram_if_cntl	Eppc405_0 LEDs_4Bit RS232_Uart r xps_bram_if_cntlr_1	0x81400000 0x8400000 0xFFFFE000	0x8140FFFF 0x8400FFFF 0xFFFFFFFF					
⊕ TestApp_Peripheral_ppc405_0	ile Location Overall I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test I:\Xilinx\Test\test	\test.xmp \test.mhs \test.mss \data\test.ucf \etc\fast_runtime.opf \etc\download.cmd \etc\bitgen.ut oc405_0 opc405_0							



## Add IP Cores

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Platform Project Files MHS File: test.mhs MIS File: test.mss UCF File: dat/test.ucf MPACT Command File: etc/download.cmd Implementation Options File: etc/fast_runtime.opt Bitgen Options File: etc/bitgen.ut Project Options Oevice: xc4vfx20ff672-10 Netlist: SubModule Implementation: Project Navigator HDL: vhdl Sim Model: BEHAVIORAL Design Summary	Name     Bus Name     IP Type     IP Version       plb     rh plb_v46     1.05.a       ppc405_0     rh processor     201.b       rh processor     rh processor     1.00.b       rh jtagppc_cnt     rh jtagppc_cntlr     2.01.c       rh processor     rh processor     1.00.b       rh jtagppc_cnt     rh processor     2.00.a       rh LEDs_4Bit     rh xps_partite     1.01.a       clock_gener     rh clock_gene     4.01.a	By Connection  By Bus Standard  By Bus Standard  Cy PLBV46  Cy OCM  Cy OCM  Cy OCR  Cy CR  Cy XILSRAM  Cy XILSRAM  Cy XILSRAM  Cy XILSRAM  Cy XILSCR  Cy XILSPOC  Cy XILSPOC  Cy XILSEETPPC  By Interface Type  Cy Slaves  Cy Master Slaves  Cy Maste
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IP Catalog	↔□₽×	Description	IP Ve	rsion
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Memory and Memory Controller			2.00	
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	🗄 IO Modules	Add IP		
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🗢 Project 📀 Applications 📀 IP Catal	e ner	VI		
	. ⊕ PCI	View IP Modifica	itions (Change Log)	
	🗄 - Peripheral Co	tr View PDF Datash	eet	
ratio ip to control ios, in this				
e. Control 5   FDs besides the	the Halles		ай 1	
		Make This IP Loo	al	
tons	Project Local PC	res		1



Ī	Р	Bus Interfaces	Ports Addre	esses		
1	L	Name		Bus Name	IP Туре	IP Version
		plb			👷 plb_v46	1.05.a
		⊕ ppc405_0			👷 ppc405_virt	2.01.b
*		plb_bram_if_cnt	lr_1_bram		🚖 bram_block	1.00.a
K		xps_bram_if_cnt	lr_1		👷 xps_bram_if	1.00.b
		🗄 jtagppc_cntlr_in	st		🚖 jtagppc_cntlr	2.01.c
	$\leftarrow$	proc_sys_reset_0	1		🐈 proc_sys_re	3.00.a
	•	南。/ FDs 4Bit			🐈 xps_gpio	2.00.a
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			Chan th <u>e n</u>	ige the name k ame.	by click once on	



🖁 Bus Inter <mark>a</mark> ces 🛛 Ports 🚽	Addre <mark>c</mark> es			Add External
Name	Net	Direction	Range	Class
🖶 External Ports 💦 🔥				
🕂 plb				
⊞ ppc405_0				
🗄 plb_bram_if_cntlr_1_bram				
⊞ xps_bram_if_cntlr_1				
jtagppc_cntlr_inst				
⊞ proc_sys_reset_0				
⊕ LEDs_4Bit				
⊞ LEDs_5Bit				
⊕ RS232_Uart				
⊞ <sup></sup> clock_generator_0				
	<u></u>			

Bus Interfaces Ports Addresses			42	Add External Port
Name	Net	Direction	Range	Class
⊕ plb				
⊕ ppc405_0				
plb_bram_if_cntlr_1_bram				
xps_bram_if_cntlr_1				
jtagppc_cntlr_inst				
proc_sys_reset_0				
D 150- 404				
⊡ LEDs_5Bit				
(BUS_IF) SPLB	Connected to BUS plb	<b>•</b>		
□ (IO_IF) gpio_0	Not connected to External Ports			
GPIO_IO_I	No Connection		[0:(C_GPIO_WID	
GPIO_IO_U	No Connection		IO:(C_GPIO_WID	
	No Connection			
	No connection	<u>▼</u> 10	[0.(C_0FIO_WID	
Hendlock generator 0				
				4
			A REAL PROPERTY AND A REAL PROPERTY.	



Bus Interfaces Ports Addresses				de la c	Add External F	Port
Name	Net		Direction	Range	Class	
Ė- External Ports						,
fpga_0_RS232_Uart_RX_pin	fpga_0_RS232_Uart_RX_pin	-	I		NONE	,
fpga_0_RS232_Uart_TX_pin	fpga_0_RS232_Uart_TX_pin		0 🗸		NONE	
fpga_0_LEDs_4Bit_GPIO_IO_pin	fpga_0_LEDs_4Bit_GPIO_IO_pin	Ŧ	IO 💌	[0:3]	NONE	
fpga_0_clk_1_sys_clk_pin	dcm_clk_s	-	I		CLK	
LED: 58: CDIO IO nin		-	10	10. <i>4</i> 1		
with the second se		•	10	[0:4]	INCINE	
⊕ ppc405 0						
plb_bram_if_cntlr_1_bram	7					Ξ
xps_bram_if_cntlr_1						
jtagppc_cntlr_inst						
proc_sys_reset_0						
🗄 LEDs_4Bit						
🖻 LEDs_5Bit						
(BUS_IF) SPLB	Connected to BUS plb	Ŧ				
🖨 (IO_IF) gpio_0	Connected to External Ports	-				
GPIO_IO_I	No Connection		I	[0:(C_GPIO_WID		
GPIO_IO_O	No Connection	Ţ	0	[0:(C_GPIO_WID		
1_01_01_0	No connection		v	[0.(C_0FIO_WID		
GPIO_IO	LEDs_5Bit_GPIO_IO	-	IO	[0:(C_GPIO_WID		-
·					Þ	

Check External Ports, they are connected automatically.
Bus Interfaces Port A	Addresses							ன Generate Address
Instance	Dase Ivame	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock	
⊨ ppc405 0's Address Map			_		Here A.			
LEDs_4Bit	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	plb		
RS232_Uart	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	plb		
xps_bram_if_cntlr_1	C_BASEADDR	0xFFFFE000	0xFFFFFFFF	8K	SPLB	plb		
e- Unmapped Addresses						4		
*		Click	and Gen	erate	addresses fo	r IPs aut	omatic	ally
Bus Interfaces Ports A	ddresses							Generate Addres
nstance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock	
⊪ ppc405_0's Address Map								
LEDs_5Bit	C_BASEADDR	0x81400000	0x8140FFFF	64K	🚽 SPLB	plb		
LEDs_4Bit	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	plb		
	C_04054000		0.01005555	C 11/				
<sup>L</sup> xps_bram_if_cntlr_1	C_BASEADDR	0xFFFFE000	0xFFFFFFFF	8K	SPLB	plb		
				8K 16K 32K 64K 128K 256K				
				512K 1M 2M 4M	~			
		Change	this IP's s	size				

#### Edit the UCF file to assign FPGA's PINs to IP's Ports

#### Xilinx Platform Studio - I:\Xilinx\Test\test\test.xmp - [test.ucf]



# Virtex 4 ML405 Evaluation Platform Net fpga 0 RS232 Uart RX pin LOC=T4 | IOSTANDARD = LVCMOS33; Net fpga 0 RS232 Uart TX pin LOC=T8 IOSTANDARD = LVCMOS33; 3 Net fpga 0 LEDs 4Bit GPIO IO pin<0> LOC=A10 | IOSTANDARD = LVCMOS25 | PULLUP SLEW = SLOW DRIVE = 5 Net fpga 0 LEDs 4Bit GPIO IO pin<1> LOC=B10 | IOSTANDARD = LVCMOS25 | PULLUP SLEW = SLOW DRIVE = 26 Net fpga 0 LEDs 4Bit GPIO IO pin<2> LOC=F13 PULLUP SLEW = SLOW IOSTANDARD = LVCMOS25 DRIVE = 2ACC 1994 C HEDS INTO OFIC TO PINCON HOC III Net LEDs 5Bit GPIO IO pin<0> LOC=G4 | 10 IOSTANDARD = LVCMOS25 PULLUP | SLEW = SLOW DRIVE = 2TIG; Net LEDs 5Bit GPIO IO pin<1> LOC=L7 | IOSTANDARD = LVCMOS25 PULLUP SLEW = SLOW DRIVE = 2TIG; 11 12 Net LEDs 5Bit GPIO IO pin<2> LOC=L9 | IOSTANDARD = LVCMOS25 | PULLUP | SLEW = SLOW DRIVE = 2TIG: 13 Net LEDs 5Bit GPIO IO pin<3> LOC=G12 | IOSTANDARD = LVCMOS25 TIG: PULLUP | SLEW = SLOW DRIVE = 214 Net LEDs 5Bit GPIO IO pin<4> LOC=E6 | IOSTANDARD = LVCMOS25 PULLUP SLEW = SLOW DRIVE = 2TIG; 15 16 Net fpga 0 clk 1 sys clk pin TNM NET = sys clk pin; 17 TIMESPEC TS sys clk pin = PERIOD sys clk pin 100000 kHz; 18 Net fpga 0 clk 1 sys clk pin LOC=AB14 | IOSTANDARD = LVCMOS33; 19 Net fpga 0 rst 1 sys rst pin TIG; 20 Net fpga 0 rst 1 sys rst pin LOC=M5 | PULLUP; 21 ###### ppc405 0 22 23 NET "ppc405 0/C405RSTCHIPRESETREQ" TPTHRU = "ppc405 0 RST GRP"; 24 NET "ppc405 0/C405RSTCORERESETREQ" TPTHRU = "ppc405 0 RST GRP"; 25 NET "ppc405 0/C405RSTSYSRESETREQ" TPTHRU = "ppc405 0 RST GRP"; TIMESPEC "TS RST ppc405 0" = FROM CPUS THRU ppc405 0 RST GRP TO FFS TIG 26 27 ш  $\Sigma$ Block Diagram System Assembly View Start Up Page Design Summary test.ucf\* х Copy these from the UCF text document in the "Documents" folder

Xilinx Platform Studio - I:\Xilinx\Test\test\test.xmp - [test.uc	.f]	
Eile Edit View Project Hardware Software Devi	ice C <u>o</u> nfi	uration Debug Simulation Window Help
	00	
	X	
		1 * VILLEX * HINDS EVALUATION FACTORM 2 Net forg 0 PS322 Tart PV in IOCET4   IOSTANDARD = IVCMOS33.
		3 Net fora 0.8532 Uart TX in LOC-16   LOSTANDARD = LVCM0533:
Description IP Version	=	
EDK Install	10	5 Net fpga 0 LEDs 4Bit GPIO IO pin<0> LOC=A10   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2
Analog	=	6 Net fpga 0 LEDs 4Bit GPIO IO pin<1> LOC=B10   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2
	=	7 Net fpga 0 LEDs 4Bit GPIO IO pin<2> LOC=F13   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2
Bus and Bridge	10	8 Net fpga 0 LEDs 4Bit GPIO IO pin<3> LOC=F14   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2
Clock, Reset and Interrupt	_	
Communication High-Speed	1	10 Net LEDs 5Bit GPIO IO pin<0> LOC=G4   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG;
Communication Low-Speed	CH4	11 Net LEDS 5Bit GPIO IO pin<1> LOC=L7   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG:
DMA and Timer	1.20	12 Net LEDS 5Bit GPIO IO pin<2> LOC=L9   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG:
🕀 Debug	24	13 Net LEDS 5Bit GPTO TO pin<3> LOC=G12   TOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG:
EPGA Reconfiguration	1 34	14 Net LEDS 5Bit GPIO TO DIC4> LOC=E6   LOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG:
General Purpose IO	1	15 Distans Studio
🕀 IO Modules		16 Net
Interprocessor Communication	i.	
Memory and Memory Controller		18 Net 2 Do you want to save the changes you made to 'data/test.uct ?
i PCI	2	
Peripheral Controller		
🕀 Processor	1	
. Utility		
Project Local PCores		22 NTT TRANSPORT (CASESTCHIDESETER) TETHEI = TREADS O DET COD.
Project Peripheral Repository0		23 NET "pro-405 0/C405RETCENTEREDENTER" = "pro-405 0 RET "pro-405 0/C405RETCENTEREDENTER
Project Peripheral Repository1		24 NEI PROHOE O/CHORACIONEREDETRES INTENNO PROHOE O ASI GRE,
		23 NAT PROTOCONTRACTOR AND A PROVIDE AND A PROVIDE AND
		21
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(0x84000000-0x8400ffff) RS232_Uart	plb	
(0xffffe000-0xfffffff) xps_bram_if_cr	atlr_1	plb
Generated Addresses Successfully		
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Save the file and close XPS, because next step we are going to add a custom IP core

## Add a custom IP Cores

Computer	► TEMP (I:) ► Xilinx ► Tutorial Materials ► UserIPs ►	5		م ر	
File Edit View Tools	Help				
Organize 👻 🔚 Open	Include in library   Share with  Burn New folder		≡ •		
🔶 Favorites	Name Date modified Type	Size			
🥃 Libraries	motor_wedge_v1_00_a 4/5/2011 10:17 AM File folder				
🤣 Homegroup					
P Computer Windows XP (C:) Windows 7 (D:) Documents (E:) Program (F:)					
TEMP (I:)					
motor_wedge_v File folder	1_00_a Date modified: 4/5/2011 10:17 AM	10-48	60% B	Mars Porto - 14	
Fi	nd the motor wedge IP in the UserIPs folder				

Include in library  Share with	Burn New folder				0
Name	Date modified	Туре	Size		
motor_wedge_v1_00_a	4/5/2011 10:20 AM	File folder			
	Name Mame Motor_wedge_v1_00_a	Name Date modified       Name     Date modified       Image: motor_wedge_v1_00_a     4/5/2011 10:20 AM	Include in inorary *     Share with *     Duth     New Torder       Name     Date modified     Type       Image: Type     Motor_wedge_v1_00_a     4/5/2011 10:20 AM     File folder	Include in library *     Snare with *     Burn     New Yolder       Name     Date modified     Type     Size       motor_wedge_v1_00_a     4/5/2011 10:20 AM     File folder	Include in libraly *     Share with *     Durn     Twee rolder       Name     Date modified     Type     Size       Image: *     Image: *     Image: *     Image: *       Image: *     Date modified     Type     Size

we add in the ISE before) in the project folder "Test".







This time we get USER IP in the list. Add three MOTOR\_WEDGE IP.

All Buses	HDL 💯 🜌
C_BASEADDR	0×fffffff
C_HIGHADDR	0x0000000
C_INCLUDE_DPHASE_TIMER	
C_SPLB_AWIDTH	32
C_SPLB_CLK_PERIOD_PS	10,000
C_SPLB_DWIDTH	128
C_SPLB_MID_WIDTH	з
C_SPLB_NATIVE_DWIDTH	32
	OK Cancel Help

	Name	Bus Name	IP Type	IP Version
	plb		👉 plb v46	1.05.a
	⊕ ppc405 0		🛉 ppc405 virt	2.01.b
11 🛏	plb_bram_if_cntlr_1_bram		gram_block	1.00.a
	xps_bram_if_cntlr_1		🐈 xps_bram_if	1.00.b
	🗄 iteanne entle inst		🚽 jtagppc_cntlr	2.01.c
	🖨 motor_wedge_0		🗧 motor_wed	1.00.a
	SPLB	plb	<b>_</b>	
	i motor_wedge_1		motor_wed	1.00.a
	SPLB	plb	<b>_</b>	
	i motor_wedge_2		🔫 motor_wed	1.00.a
	SPLB	plb	<b>_</b>	
	proc_sys_reset_0		👷 proc_sys_re	3.00.a
	ia LEDs_4Bit		y xps_gpio	2.00.a
	The start of the s		👷 xps_gpio	2.00.a
	B RS232_Uart		👷 xps_uartlite	1.01.a
	···· clock_generator_0		ή clock_gene	4.01.a
	•	III		
aster ●Slave ● roduction BLic uperseded O	Master/Slave > Target <initiator ense (paid)</initiator 	Connected OUnc	onnected M Monitor duction ®Beta ZDev	elopment
Start Up Page	e 🔣 🗵 Design Summary	🔣 😎 🛛 Block 🛙	Diagram 🛛 📀 S	ystem Assembly View 🛛 📋
	Connect these th	ree MOTOR V	VEDGE IP to pll	o bus.

			e		
Name	Net	Direction	Range	Class	1
⊕~ppc405_0					
🗄 plb_bram_if_cntlr_1_bram					
⊕ xps_bram_if_cntlr_1					
jtagppc_cntlr_inst					
imotor_wedge_0					
(IO_IF) motorwedge_0	Connected to External Ports	<b>•</b>			
	······································				
ENCB1	motor_wedge_0_ENCB1	• I			
ENCA2	motor_wedge_0_ENCA2	💌 I			1
ENCB2	motor_wedge_0_ENCB2	\star I			
EN1	motor_wedge_0_EN1	<b>→</b> 0			
EN2	motor_wedge_0_EN2	<b>→</b> 0			
INA1	motor_wedge_0_INA1	<b>→</b> 0			
···· INB1	motor_wedge_0_INB1	<b>U</b>			
···· INA2	motor_wedge_0_INA2	<b>→</b> 0			
INB2	motor_wedge_0_INB2	🖵 O			
motor_wedge_1					
(BUS_IF) SPLB	Connected to BUS plb	•			
IO_IF) motorwedge_0	Connected to External Ports	<b>.</b>			
⊡…motor_wedge_2					
(BUS_IF) SPLB	Connected to BUS plb	<b>•</b>			
•					P
legend					
Master 🎱 Slave 🕋 Master/Slave 🕨 Ta	irget <initiator ounconnec<="" td="" 🧕connected=""><td>ted M Monitor</td><td></td><td></td><td></td></initiator>	ted M Monitor			
Production 🗟 License (paid) 🛛 🚳 Lic	cense (eval) 🗆 🗟Local 🚢Pre Productio	n 🚯 Beta 🗮 Developm	ient		
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	• • • • • • • •			ALC:	
	Connact thair norts to avta	rnal norts			

Bus Interfaces Ports Addresses				🚓 Add External P
Name	Net	Direction	Range	Class
External Ports				
fpga 0 RS232 Uart RX pin	fpga 0 RS232 Uart RX pin	▼ I	-	NONE
fpga_0_RS232_Uart_TX_pin	fpga 0_RS232_Uart_TX_pin	<b>v</b> 0	<b>T</b>	NONE
fpga_0_LEDs_4Bit_GPIO_IO_pin	fpga_0_LEDs_4Bit_GPIO_IO_pin	V IO		NONE
fpga_0_clk_1_sys_clk_pin	dcm_clk_s	▼ I	<b>T</b>	CLK
fpga_0_rst_1_sys_rst_pin	sys_rst_s	▼ I	-	RST
- LEDs 5Bit GPIO IO pin	LEDs 5Bit GPIO IO	- 10	- 10:41	NONE
motor_wedge_0_ENCA1_pin	motor_wedge_0_ENCA1	▼ I	-	NONE
	motor_wedge_0_ENCB1	▼ I	-	NONE
motor_wedge_0_ENCA2_pin	motor_wedge_0_ENCA2	▼ I	-	NONE
motor_wedge_0_ENCB2_pin	motor_wedge_0_ENCB2	▼ I	-	NONE
motor_wedge_0_EN1_pin	motor_wedge_0_EN1	<b>v</b> 0	-	NONE
motor_wedge_0_EN2_pin	motor_wedge_0_EN2	<b>v</b> 0	-	NONE
motor_wedge_0_INA1_pin	motor_wedge_0_INA1	<b>v</b> 0	-	NONE
motor_wedge_0_INB1_pin	motor_wedge_0_INB1	<b>v</b> 0	-	NONE
motor_wedge_0_INA2_pin	motor_wedge_0_INA2	<b>v</b> 0	-	NONE
motor_wedge_0_INB2_pin	motor_wedge_0_INB2	<b>v</b> 0	-	NONE
motor_wedge_1_ENCA1_pin	motor_wedge_1_ENCA1	▼ I	-	NONE
motor_wedge_1_ENCB1_pin	motor_wedge_1_ENCB1	▼ I	-	NONE
motor_wedge_1_ENCA2_pin	motor_wedge_1_ENCA2	▼ I	<b>_</b>	NONE
motor_wedge_1_ENCB2_pin	motor_wedge_1_ENCB2	V I	<b>_</b>	NONE
motor wedge 1 EN1 pin	motor wedge 1 EN1	<b>0</b>		NONE
•				F
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Bus Interfaces Ports	Addresses								🚟 Generate Addresses			
Instance	Base Name	Base Address	High Address	Size	Bus Inter	face(s) Bus	Name Loo	k				
- → ppc405 0's Address Map												
LEDs 5Bit	C BASEADD	R 0x81400000	0x8140FFFF	64K	SPLB	plb						
LEDs 4Bit	C BASEADD	R 0x81420000	0x8142FFFF	64K	- SPLB	plb						
RS232 Uart	C BASEADD	R 0x8400000	0x8400FFFF	64K	SPLB	plb						
xps bram if cntlr 1	C BASEADD	R OxFEFE0000	OXEFFEFEF	128K	SPLB	plb						
Unmapped Addresses						P	<u> </u>					
		-	-			1						
		(	Bus Interfaces	Ports A	aaresses							Generate Addres
			Instance		Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock	
			⊨ ppc405_0's Addre	ess Map								
			LEDs_5Bit		C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	plb		
			LEDs_4Bit		C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	plb		
			RS232_Uart		C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	plb		
			motor_wedg	2	C_BASEADDR	0xC2400000	0xC240FFFF	64K	SPLB	plb		
			motor_wedge	1	C_BASEADDR	0xC2420000	0xC242FFFF	64K	SPLB	plb		
			motor_wedge	20	C_BASEADDR	0xC2440000	0xC244FFFF	64K	SPLB	plb		
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<u>File Edit View Project Hardware</u>	Software Device C	e C <u>o</u> nfiguration D <u>e</u> bug S <u>i</u> mulation <u>W</u> indow <u>H</u> elp	_ & ×
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IP Catalog	↔□₽×	X = 12 Net LEDs 5Bit GPTO TO pin<2> LOC=L9   TOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = :	2   TIG: 🔺
		T 13 Net LEDs 5Bit GPIO IO pin<3> LOC-G12   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE =	2   TIG;
Description	IP Version	14 Net LEDs 5Bit GPIO IO pin<4> LOC=E6   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2	2   TIG;
🖨 灯 EDK Install			
+ Analog		1 Net motor_wedge_0_ENCA1_pin_LOC=AD20   IOSTANDARD = LVCMOS33;	
Arithmetic		7 Net motor wedge 0 EN1 pin LOC=Y23   IOSTANDARD = LVCMOS33;	
🕀 Bus and Bridge		18 Net motor wedge 0 INAI pin LOC=V24   LOSIANDARD = LVCMOS33;	
Clock, Reset and Interrupt		2 19 Net motor wedge _ ENG82 pin LOC=W23   LOSTANDADD = LVGMOS33;	
Communication High-Speed			
Communication Low-Speed	5	22 Net motor wedge 0 ENCB1 pin LOC=AA22   IOSTANDARD = LVCMOS33;	
DMA and Timer		23 Net motor wedge 0 INB1 pin LOC=Y22   IOSTANDARD = LVCMOS33;	E
⊕ Debug		24 Net motor wedge 0 ENCA2 pin LOC=AC18   IOSTANDARD = LVCMOS33;	
FPGA Reconfiguration		25 Net motor wedge 0 EN2 pin LOC=AC19   IOSTANDARD = LVCMOS33;	
General Purpose IO		26 Net motor_wedgeINA2_pin LOC=Y18   IOSTANDARD = LVCMOS33;	
Interprocessor Communication		27	
Memory and Memory Controller		28 Net motor_wedge_1_ENCA1_pin LOC=V23   IOSTANDARD = LVCMOS33;	
PCI	-	29 Net motor_wedge_1_EN1 pin LOC=U24   IOSTANDARD = LVCMOS33;	
Peripheral Controller		30 Net motor_wedge 1 INA1 pin LOC=T23   IOSTANDARD = LVCMOS33;	
Processor		31 Net motor wedge 1 ENGE2 pin LOC=124   IOSTANDARD = LVCM0533;	
🕀 Utility		32 Net motor_wedge_1_Nb2_pin Loc-k23   1051ANDARD - Loch0553;	
Project Local PCores		34 Net motor wedge 1 ENCB1 pin LOC=2018   TOSTANDARD = LVCMOS33.	
⊡ USER		35 Net motor wedge 1 INB1 pin LOC=ACI6   IOSTANDARD = LVCMOS33;	
	1.00.a	36 Net motor wedge 1 ENCA2 pin LOC-AD16   IOSTANDARD - LVCMOS33;	
		37 Net motor wedge 1 EN2 pin LOC=T18   IOSTANDARD = LVCMOS33;	
		18 Net motor_wedge_1_INA2_pin LOC=U19   IOSTANDARD = LVCMOS33;	
			-
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🔶 Project 🔶 Applications 🔶 IP Catalo	g	🔶 Start Up Page 🗵 🗵 Design Summary 🗵 🔶 Block Diagram 🔝 🔶 System Assembly View 🗵 📄 test.ucf* 🗵	
Console			⇔⊡₽×
(0xc2440000-0xc244ffff) mot	or_wedge_0 plt	plb	*
(Oxfffe0000-Oxffffffff) xps	_bram_if_cntlr	clr_1 plb	
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Stiller Faite View Designt Unselvere Coffeener	Device Confi	Francisco Dalvar Considerina Mindeus Hele	
	Device Conii		
	( ( ) ) ( ) ( ) ( ) ( ) ( ) ( ) ( ) ( )		
IP Catalog ++	08× 💽	12 Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 1	2   TIG; 🔺
t <mark>:</mark> ●	Þ	13 Net LEDs_Shit_GPI0_I0_pin<3> LOC=G12   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE =	2   TIG;
Description IP Version	on	14 Net LEDS_5Bit_GPIO_IO_pin<4> LOC=E6   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE =	2   TIG;
🖨 🐔 EDK Install	=	16 Net motor wedge 0 ENCA1 pin LOC=AD20   LOSTANDARD = LVCM0533:	
	1	17 Net motor wedge 0 EN1 pin LOC=Y23   IOSTANDARD = LVCMOS33;	
Arithmetic	Ξ.	18 Net motor_wedge_0_INA1_pin LOC=V24   IOSTANDARD = LVCMOS33;	
Bus and bridge	10	19 Net motor_wedge_0_ENCB2_pin LOC=W23   IOSTANDARD = LVCMOS33;	
Communication High-Speed		- 20 Net motor_wedge_0_INB2_pin LOC=V22   IOSTANDARD = LVCMOS33;	
Communication Low-Speed	. ^		
DMA and Timer	*	22 Net motor_wedge_0_INET_pin_LOC-AA22   IOSTANDARD = LOCMOSSS;	E
⊕ Debug	*	24 Net motor wedge 0 ENCA2 pin LOC=AC18   IOSTANDARD = LVCMOS33;	1
PPGA Reconfiguration	*	25 Net motor_wedge_0_EN2_pin_LOC=AC19   IOSTANDARD = LVCMOS33;	
General Purpose IO	1	26 Net motor_wedge_0_INA2_pin LOC=Y18   IOSTANDARD = LVCMOS33;	
Interprocessor Communication		27	
Memory and Memory Controller	1	28 Net motor_wedge_1_ENCA1_pin_LOC=V23   IOSTANDARD = LVCMOS33;	
⊕ PCI		29 Net motor wedge 1 ENI pin LOC=U24   IOSIANDARD = LVCROS33;	
Peripheral Controller		30 Net motor wedge 1 ENCE pin LOC-125   IOSTANDARD = LVCMOS33;	
Processor	-	32 Net motor wedge 1 INB2 pin LOC=R23   IOSTANDARD = LVCMOS33;	
Design to a set D Course		33	
	_	34 Net motor_wedge_1_ENCB1_pin LOC=AA18   IOSTANDARD = LVCMOS33;	
MOTOR WEDGE 1.00.a		35 Net motor_wedge_1_INB1 pin LOC=AC16   IOSTANDARD = LVCMOS33;	
		36 Net motor wedge 1 ENCA2 pin LOC-ADI6   IOSTANDARD = LVCMOS33;	
		38 Net motor wedge 1 INA2 pin LOC-U19   LOSTANDARD = LVCMOS33;	
		39	_
•	•	4 mm	- F
🗢 Project 🐟 Applications 🐟 IP Catalog		🔪 Start Up Page 🛛 🔀 Design Summary 🔀 😚 Block Diagram 🖂 😚 System Assembly View 🗶 📄 test.ucf* 🔲	
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		IDe is some plated. Fult VDC and we head to ICF	
AC	laing	TPS IS COMPLETED. EXIL XPS and go back to ISE.	
	5		

# Part IV: Create a Software Project in SDK

This part will show you how to actually put some codes in this project and run it in FPGA.

ISE Project Navigator (M.81d) - I:\Xilinx\Test\Test.xise		Name of Concession, Name		
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Before opening	SDK we need	to export hardwa	re design to it in ISE	
Berore opening				



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File nam	e: test.ucf	✓ Sources(*.txt *.vhd *.vhdl *.v *.l	-
		Open Cancel	
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The UCF file is under the "data" folder in the "test" (embedded core) of the project folder "Test".





Design	↔□₽× 🔳	1	# Virtex 4 ML405 Evaluation Platform	
📑 View: 💿 🔯 Implementation 🔘 🎆 Simulation	<u>6</u>	2	Net fpga_0_RS232_Uart_RX_pin LOC=T4	IOSTANDARD =
		3	Net fpga_0_RS232_Uart_TX_pin LOC=T8	IOSTANDARD =
	<b>=</b>	4		
👔 🖶 🕘 Test	10	5	Net fpga_0_LEDs_4Bit_GPI0_I0_pin<0> LOC	=A10   IOSTZ
⊡ xc4vfx20-10ff672		6	Net fpga_0_LEDs_4Bit_GPI0_I0_pin<1> LOC	=B10   IOSTA
test (test.xmp)	=	7	Net fpga_0_LEDs_4Bit_GPI0_I0_pin<2> LOC	=F13   IOSTA
test.ucf	10	8	Net fpga_0_LEDs_4Bit_GPI0_I0_pin<3> LOO	C=F14   IOSTZ
	_	9		
673 I	1	10	Net LEDs_5Bit_GPI0_I0_pin<0> LOC=G4	IOSTANDARD =
	56	11	Net LEDs_5Bit_GPIO_IO_pin<1> LOC=L7	IOSTANDARD =
	1	12	Net LEDs_5Bit_GPI0_I0_pin<2> LOC=L9	IOSTANDARD =
	; 7%-	13	Net LEDs_5Bit_GPI0_I0_pin<3> LOC=G12	IOSTANDARD =
ш	: **	14	Net LEDs_5Bit_GPI0_I0_pin<4> LOC=E6	IOSTANDARD =
		15		
		16	Net motor_wedge_0_ENCA1_pin LOC=AD20	IOSTANDARD =
Running: Platform Generator		17	Net motor_wedge_0_EN1_pin LOC=Y23   1	OSTANDARD = LV
Processes: test	-	18	Net motor_wedge_0_INA1_pin LOC=V24	IOSTANDARD = I
		19	Net motor_wedge_0_ENCB2_pin LOC=W23	IOSTANDARD =
Design Summary/Reports		20	Net motor_wedge_0_INB2_pin LOC=V22	IOSTANDARD = I
Bill B. Weer Constraints		21		
Supplier VST		22	Net motor_wedge_0_ENCB1_pin LOC=AA22	IOSTANDARD =
June Synchesize - AST		23	Net motor_wedge_0_INB1_pin LOC=Y22	IOSTANDARD = I
Generate Programming File		24	Net motor_wedge_0_ENCA2_pin LOC=AC18	IOSTANDARD =
Configure Target Device		25	Net motor_wedge_0_EN2_pin LOC=AC19	IOSTANDARD = I
		26	Net motor_wedge_0_INA2_pin LOC=Y18	IOSTANDARD = I
Export Hardware Design To SDK		27		
CH Archer Design 10 3DK		28	Net motor_wedge_1_ENCA1_pin LOC=V23	IOSTANDARD =
		•		
📨 Start 🖳 Design 🖺 File, 🚺 Libraries			test.ucf	
Casaala				

Double click on it to export hardware design to SDK. This might take several minuets.

ISE Project Navigator (M.81d) - I:\Xilinx\Test\Test.xise - [test.ucf]	Table House Here	
<u>File Edit View Project Source Process Tools Window</u>	Layout <u>H</u> elp	_ <del>_</del> <del>_</del> <del>_</del>
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Design ↔ □ ₽ ×	1 # Virtex 4 ML405 Evaluation Platform	
View:  View:  Kinder in the implementation  Kinder in the implemen	2 Net fpga_0_RS232_Uart_RX_pin_LOC=T4   IOSTANDAI 3 Net fpga_0_RS232_Uart_TX_pin_LOC=T8   IOSTANDAI 4 5 Net fpga_0_LEDs_4Bit_GPI0_I0_pin<0>_LOC=A10   : 6 Net fpga_0_LEDs_4Bit_GPI0_I0_pin<1>_LOC=B10   :	RD = LVCMOS33; RD = LVCMOS33; IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2
	<pre>7 Net fpga_0_LEDs_4Bit_GPI0_I0_pin&lt;2&gt; LOC=F13   8 Net fpga_0_LEDs_4Bit_GPI0_I0_pin&lt;3&gt; LOC=F14   9 10 Net LEDs_5Bit_GPI0_I0_pin&lt;0&gt; LOC=G4   IOSTANDAN</pre>	IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   E IOSTANDARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   E RD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG;
	11 Net LEDs_5Bit_GPIO_IO_pin<1> LOC=L7   IOSTANDAJ 12 Net LEDs_5Bit_GPIO_IO_pin<2> LOC=L9   IOSTANDAJ 13 Net LEDs_5Bit_GPIO_IO_pin<3> LOC=G12   IOSTANDAJ 14 Net LEDs_5Bit_GPIO_IO_pin<4> LOC=E6   IOSTANDAJ 15	RD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG; RD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG; ARD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG; RD = LVCMOS25   PULLUP   SLEW = SLOW   DRIVE = 2   TIG;
Opening: test.xmp	16 Net motor_wedge_0_ENCA1_pin_LOC=AD20   IOSTANDA 1 Net motor_wedge_0_EN1_pin_LOC=Y23   IOSTANDARD	ARD = LVCMOS33; = LVCMOS33;
Processes: test	18 Net motor_wedge_0_INA1_pin_LOC=V24   IOSTANDAR	D = LVCMOS33;
👷 📃 Design Summary/Reports	<pre>19 Vet motor_wedge_0_ENCB2_pin LOC=W23   IOSTANDAN 20 Net motor wedge 0 INB2 pin LOC=W22   IOSTANDAN</pre>	RD = LVCMOS33; D = LVCMOS33;
Using Utilities User Constraints User Constraints Synthesize - XST Implement Design Generate Programming File Configure Target Device Update Bistream with Processor Data Export Hardware Design To SDK Analyze Design Using ChipScope	<pre>21 22 Net motor_wedge_0_ENCB1_pin_LOC=AA22   IOSTANDA 23 Net lotor_wedge_0_INB1_pin_LOC=Y22   IOSTANDAR 24 Net motor_wedge_0_ENCA2_pin_LOC=AC18   IOSTANDAR 25 Net motor_wedge_0_ENC2_pin_LOC=AC19   IOSTANDAR 26 Net motor_wedge_0_INA2_pin_LOC=Y18   IOSTANDAR 27 28 Net motor_wedge_1_ENCA1_pin_LOC=V23   IOSTANDAR 4 11 11 12 12 13 14 14 14 14 14 14 14 14 14 14 14 14 14</pre>	ARD = LVCMOS33; D = LVCMOS33; ARD = LVCMOS33; D = LVCMOS33; D = LVCMOS33; RD = LVCMOS33;
Start Design C Files C Libraries	test.ucf	
Console		↔□₽×
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Wh	en export process is done, dou	ble click on the test.xmp

to open XPS.







we exporting hardware design to it in ISE.

### Create a Software Project

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		📅 Header File		
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2	Refresh F5			Watch a short SDK screencast.
	Convert Line Delimiters To	D Other Ctrl+N		► Watch Now
Ð	Print Ctrl+P	Name: standalone		E
	Switch Workspace	Version: 3.00.a		Getting Started
	Posted	ription: Standalone is a simple, low-level software layer.	It provides access to basic processor features such as basic features of a hosted environment, such as	<ul> <li>Cotting Started with Villar SDK</li> </ul>
	Nestan	standard input and output, profiling, abort and e	exit.	EDK Concepts Tools and Technic
2	Import	ntation: <u>standalone v3 00 a</u>		Migrating from SDK 11.x
4	Export			Frequently asked questions
	Properties Alt+Enter	al Drivers		Known laguag
		resent in the Board Support Package.	<b>T</b>	Known issues
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ocation: I:\Xilinx\Te	est\test\SDK\SDK_Work	space_35\hello_world_0	Browse	
Target Hardware				
Hardware Platform:	hw_platform_0			
Processor:	ppc405_0			
Select Project Temp	late			
Dhystone		Description		
Empty Application		Let's say 'Hello World' in C.	*	
IwIP Echo Server				
Peripheral Tests				
SREC Bootloader Xilkernel POSIX Thr	eads Demo			Section 2
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Hardware Platform: Processor:	hw_platform_0 ppc405_0			Put the name of the project here.
Dhrystone Empty Application Hello World IwIP Echo Server Memory Tests Peripheral Tests SREC Bootloader Xilkernel POSIX Thre	eads Demo	Description A blank C project.		
?		< <u>B</u> ack <u>N</u> ext > <u>F</u> ir	nish Cancel	

Create a managed make app	ication project. Choose from one of the sample applications.	G	
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The template provided b	application 'Empty Application' will be used to configure the p	oroject.	
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Use <u>d</u> efault location			
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Target an existing Board Su	ipport Package		Same thing. But do
Available Board Support P	ackages:		leave _usp_u liere





Copy the codes under the folder "test" in the "Function Codes" folder.



Paste these files here at "src" folder under the C project we built(test\_0).



Build the project by saving it or some other ways. We will get .elf file which is to be downloaded into the FPGA.



Download our project into the FPGA by this option.
Specify the bitstream and the ELF files that reside in BRAM memory         Hardware Configuration         Hardware Specification: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.xml         Bitstream:       I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system.bit         Browse         BMM File:       I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system_bd.bmm         Browse         Software Configuration         Processor       EL F File to Initialize in Block RAM         ppc405_0       bc otloop         Program       Cancel	rogram FPGA			→
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BMM File: I:\Xilinx\Test\test\SDK\SDK_Workspace_35\hw_platform_0\system_bd.bmm   Software Configuration   Processor   EI   F File to Initialize in Block RAM   ppc405_0   bc otloop     Program     Cancel	Bitstream: I:\Xilinx\	Test\test\SDK\SDK_Workspace_35	hw_platform_0\system.bit	Browse.
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Software C	onfiguration				
Processor ELF File to Initialize in Block RAM					
ppc405_0	I:\Xilinx\Test\test\SDK\SDK_Workspace_35\test_0\De 👻				
	I:\Xilinx\Test\test\SDK\SDK_Workspace_35\test_0\Debug\test_0.elf				
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Program I	FPGA	2-0-	
Specify the	bitstream and the ELF files that reside in BRAM memory		
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Processor	ELF File to Initialize in Block RAM		
ppc405_0	I:\Xilinx\Test\test\SDK\SDK_Workspace_35\test_0\De		
?	Program	Cancel	



## Result

First, two sets of LEDs on the ML405 should be blinking. Then some message should be sent through UART to your PC.

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	Testing		g
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Open your hyper-terminal or something like it. Chose the com you connected and set Baud Rate as 9600. Details about it can be found in the property of the uart IP core in XPS.