Tutorial of How to Use PROM (xcf32p) on RecoNode (TRC1000)

- Start -> All Programs -> ISE Xilinx Design Suite 13.2 -> ISE Design Tools -> Tools -> iMPACT (open iMPACT)
- 2. Cancel all firstly. File -> New Project, choose "Yes" when a window popped up.

ISE iMPACT (0.61xd) - D:\Xilinx\13.2\ISE_DS\a	auto_project.ipf - [Bound	ary Scan]	States Laboration	the Manual Real	
Eile Edit View Operations Output	Debug <u>W</u> indow <u>H</u> e	lp			- 8 ×
New Project Ctrl+N	i 🖉 🗟 🗉	<i>₽</i> k ?			
🙀 ờ Open P <u>r</u> oject Ctrl+O					
Open Configuration Archive Ctrl+H	_				
10 Initialize Chain Ctrl+1		Extra:			
Save Project Ctrl+S					
Save Project As Ctrl+J	xcf32p	xc4vfx20			
Save Configuration Archive	bypass	bypass			
Export Project To CDF					
Recent Files					
New Log File					
Exit					
	_				
Available Operations are:					
i Erase					
Blank Check					
Get Device ID					
Get Device Checksum					
- occounce signature osciedae					
				Identify Succeeded	
	%	Boundary Scan	\$	Boundary Scan	
Console					+ □ 8 ×
PROGRESS_END - End Operation.					*
Elapsed time = 0 sec. // *** BATCH CMD : identifyMPM					
					•
< m					Þ
Errors 🔝 Warnings					
Create a new project IPF file					Configuration Platform Cable USB 6 MHz usb-hs
🐸 o 🛛 🔚 O	- 😵 🕓	📼 🙆 🧉 🖉	👜 🍇 🎭 –		EN 🔺 💑 🍫 🔐 .all 🌒 1:23 PM

3. Click "Create PROM File"



 Click "Xilinx Flash/PROM" -> green arrow -> in Device choose 'xcf32p' -> Add storage Device -> green arrow -> Change name in "Output File Name" -> Change save location in "Output File Location" -> Click "OK"

PROM The Formatter							e	
Step 1. Select Storage Target	t	Step 2. Add	l Storage Device(s)		Step 3.		Enter Da	ata
Storage Device Type :]	DDOM Englis	Diatform Flash		General File Detail		Value	
Xilinx Flash/PROM		Device (bits)	xcf32p [32 M]		Checksum Fill Value	FF		
Spartan3AN		Add Storage Device	Remove Storage Device		Output File Name	DU100_PROM	_TEST	
Configure Single FPGA Configure MultiBoot FPGA		xcf32p [32 M]			Output File Location	D:\Xilinx\13.2\ISE_DS\		0
Configure Single FPGA Configure MultiBoot FPGA					Flash/PROM Fil	e Property	Value	
Configure from Paralleled PROMs				-	File Format		MCS	-
Generic Parallel PROM					Enable Revisioning		Yes	•
					Number Of Revision	ns	1	•
					Enable Compression	n	No	•
		Auto Select PROM						
Description:								
The PROM File Formatter will guide you through the steps to format bitstream BIT files into a PROM file that is compatible with Xilinx® and third-party PROM programmers. The programmed PROM device can then be used to configure the target FPGA.								
Additional capabilities of the PROM File Formatter include								
Generation DP/DM files containing creditis EPGA configuration instructions required to support daisu-chained EPGA bitetraam RIT files								
					<u>O</u> K	Can	cel Hel;	,

5. Cancel all firstly. Then right click on xc4vfx20 -> Assign New Configuration File, browse to the "download.bit" directory from

"DU100_PROM_Demo_Tutorial\DU100_PROM_test_13.2\SDK\SDK_Export\DU100_PRO M_test_hw_platform"



Then click "Generate File" at left bottom panel.

6. Right click on xcf32p -> Assign New Configuration File, browse to the directory of .mcs file you saved in step 4.

SE iMPACT (0.61xd) - D:\Xilinx\13.2\ISE_DS	auto_project.ipf - [Bou	indary Scan]	successive fragment store of	Record Red	
le Edit View Operations Output	Debug Window	Help			_ # ×
🗋 🏓 🛃 🐰 🖻 📮 🗙 🖽 🖽 😫	💥 il 🥏 📑 🗔	<i>₽</i> k?			
MPACT Processes MPACT Processes MPACT Processes Method MPACT Method Method MPACT Method MPACT Method Method Method Method MPACT Method Method Method MPACT Method Method MPACT Method Method MPACT Method Method Method Method MPACT Method Meh	TDI ZUM xcf3 TDO byp4	Example Erse Blank Check Readback Get Device Dio Get Device Signature/Usercode Assign New Configuration File Set Programming Properties Est Programming Properties Launch File Assignment Wicard			
	8	Boundary Scan	8	PROM File Formatter	
Console					+□8×
Project: 'D:\Xilinx\13.2\ISE Cable is not connected.	D of Report DS\\auto_projec	t.ipf' loaded.			^
Errors 🔬 Warnings					No Cable Comparison No File Open
					INO Cable Connection No File Open
	🔜 🥝 🕟				EN 🔺 💑 🍫 🔐 💷 🕪 1:33 PM

 Right click on xcf32p -> Set Programming Properties , make sure the configuration of PROM is like the following figure.

ISE iMPACT (0.61xd) - D:\Xiiinx\13.2\ISE_DS	auto_project.ipf - [Boundary Scan]	state international distance in the second state			
Bile Edit View Operations Qutput	Debug Window Help			- 8 ×	
🗋 🏓 🛃 🕺 🛍 ն 🗙 🔠 🗊	x ii # # 🖉 🗢 🖪 🔑 K?				
MPACT Flows ↔ □ & ×					
Beundary Scan Control	TDI Program Yerly Erse tase Blink Check Beadback Get Device Dip Get Device Signature/Usercode Get Device Signature/Usercode Get Device Signature/Usercode Get Device Signature/Usercode Get Device Colloguation Revision Qne Step SVF One Step SVF One Step SVF Assign New Configuration File Set Programming Properties Set Erse Properties				
 Load Configuration Revision One Step SVF 					
One Step XSVF	Boundary Sca	n			
Console				++ □ @ X	
done.) INFO:IMPACT:1835 - Loading CF // *** BAICH CMD : setAttribu ("" Console Errors 1 Warnings	file Cr/Users/YanzheCui/Desktop/DUIO0_ e -position 1 -attr packageName -value *	ROM_Demo_Tutorial/MCS file for FROM/DUl00_FROM_TEST.of	fi	Platform Cable 1150 16 Adds [] June be	
🔊 o o 🔽 o			EN	Antoin Cable 038 (0 Min2 1 136 PM	
PROM Specific Pro	perties				
Load FPGA					
Parallel Mode					
Advanced PROM R	Programming Properties	;			
During Configurat	ion: PROM is Configurat	tion Master (check to select cloc	ck source)		
	[select cl	ock source]		External Clock	-
During Configurat	ion: PROM is Slave (cloc	ked externally)		V	

8. Right click on xcf32p -> Program